


Reference Schematic For RK3399Pro

RK3399Pro_AI_REF_V11_20190520

PMIC: RK809-3 (5BUCK + 9LDO + Codec)
CPU RAM: LPDDR3/DDR3L/LPDDR4
NPU RAM: LPDDR3/DDR3L
ROM: eMMC + Micro-SD(TF) card
Interface: MIPI CSI/MIPI DSI/UART/I2S/RGMII/USB2.0/TYPER-C/HDMI/EDP

		Fuzhou Rockchip Electronics	
瑞芯微电子			
Project:	RK3399Pro AI REF V11		
File:	00.Cover Page		
Date:	Tuesday, May 21, 2019		Rev: V1.1
Designed by:	Linus.Lin	Reviewed by: <Checker>	Sheet: 1 of 46

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Note

NOTE 1:

Component parameter description

1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:

Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Bill of Materials

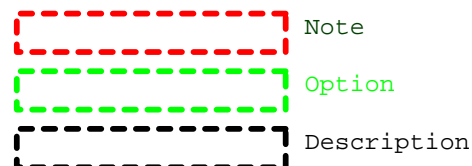
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Item\Part\Description\PCB Footprint\Reference\Quantity\Option

Combined property string:

{Item}\{Value}\{Description}\{PCB Footprint}\{Reference}\{Quantity}\{Option}

Graphic Description



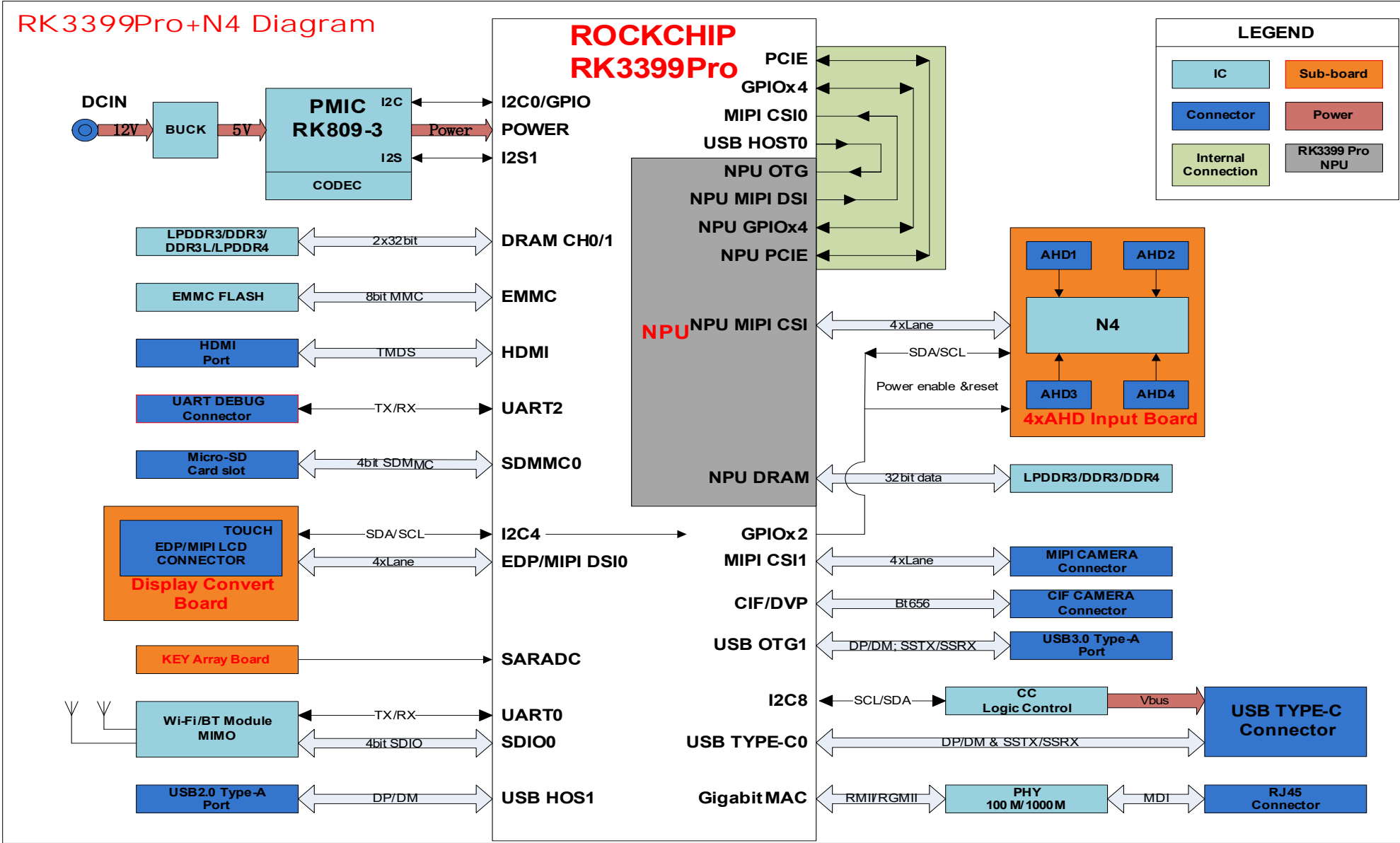
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Project:	RK3399Pro AI REF V11				
File:	01.Index				
Date:	Tuesday, May 21, 2019			Rev:	V1.1
Designed by:	Linus.Lin	Reviewed by:	<Checker>	Sheet:	2 of 46

Revision History


Version	Date	Author	Change Note	Approved
V1.0	2018.11.22	RZF	First edition for RK3399Pro	CHENW
V1.1	2019.05.20	Linus.Lin	1.Add NPU MIPI-CSI for N4 connection. 2.Add NPU MIPI-DSI for CPU connection。 3.Add DDR4/LPDDR2 interface for NPU DDR Ctrl.. 4.Modify the connection mode between CPU and NPU from USB3.0 to PCIE. 5.Delete net connection of VCC_DDRC. 6.Delete Touch COB module. 7.Modification and optimization.	CHENW

RK3399Pro Block Diagram



I2C MAP

Port	Pin Name	Domain	Bus Name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Slave Bus Capability	Note
I2C0	I2C0_SCL/GPIO1_C0_u I2C0_SDA/GPIO1_B7_u	PMUIO2	I2C0_SCL_PMIC I2C0_SDA_PMIC	VCC_1V8_S3	RK809-3	0x20	100kHz,400kHz	Rockchip PMIC
					TCS4525	0x1c	100kHz,400kHz,3.4MHz	Torch-chip DC-DC BUCK
					TCS4526	0x10	100kHz,400kHz,3.4MHz	Torch-chip DC-DC BUCK
I2C1	I2C1_SCL/GPIO4_A2_u I2C1_SDA/GPIO4_A1_u	APIO5	I2C1_SCL_1V8 I2C1_SDA_1V8	VCC_1V8_S0	CAMERA	N/A	100kHz,400kHz	MIPI/CIF CAMERA
					MPU6500	0x68	100kHz,400kHz	InvenSense Gyroscope+G-sensor
					AK8963C	0x0d	100kHz,400kHz	AsahiKASEI COMPASS
I2C2	I2C2_SCL/GPIO2_A1_u I2C2_SDA/GPIO2_A0_u	APIO2	NC					
I2C3	I2C3_SCL/GPIO4_C1_u I2C3_SDA/GPIO4_C0_u	APIO4	I2C3_SCL_HDMI I2C3_SDA_HDMI	VCCIO_3V0_S0	HDMI	N/A	100kHz,400kHz	HDMI
I2C4	I2C4_SCL/GPIO1_B4_u I2C4_SDA/GPIO1_B3_u	PMUIO2	I2C4_SCL_TP I2C4_SDA_TP	VCC_1V8_S3	N4	0x30	100kHz,400kHz	Nextchip 4-AHD
					Touch IC	N/A	100kHz,400kHz	Touch IC
I2C5	I2C5_SCL/GPIO3_B3_u I2C5_SDA/GPIO3_B2_u	APIO1	NC					
I2C6	I2C6_SCL/GPIO2_B2_u I2C6_SDA/GPIO2_B1_u	APIO2	NC					
I2C7	I2C7_SCL/GPIO2_B0_u I2C7_SDA/GPIO2_A7_u	APIO2	NC					
I2C8	I2C8_SCL/GPIO1_C5_u I2C8_SDA/GPIO1_C4_u	PMUIO2	I2C8_SCL_CC I2C8_SDA_CC	VCC_1V8_S3	ET302Y FUSB302B	0x40,0x46	100kHz,400kHz,1MHz	ETEK USB Type-C Mux Fairchild USB Type-C Mux
NPU I2C1	NPU_I2C1_SCL/GPIO0_C0_u NPU_I2C1_SDA/GPIO0_C1_u	NPU_VCC_1V8	NPU_I2C1_SCL NPU_I2C1_SDA	NPU_VCC_1V8_S3	TCS4525	0x1c	100kHz,400kHz,3.4MHz	Torch-chip DC-DC BUCK
NPU I2C3	NPU_I2C3_SCL/GPIO2_D0_u NPU_I2C3_SDA/GPIO2_D1_u	NPU_VCC_1V8_S3	NPU_I2C3_SCL NPU_I2C3_SDA	NPU_VCC_1V8_S3	CAMERA	N/A	100kHz,400kHz	CIF CAMERA



Fuzhou Rockchip Electronics

Project:

RK3399Pro AI REF V11

File:

04.I2C MAP

Date:

Tuesday, May 21, 2019

Designed by:

Linus.Lin

Reviewed by:

<Checker>

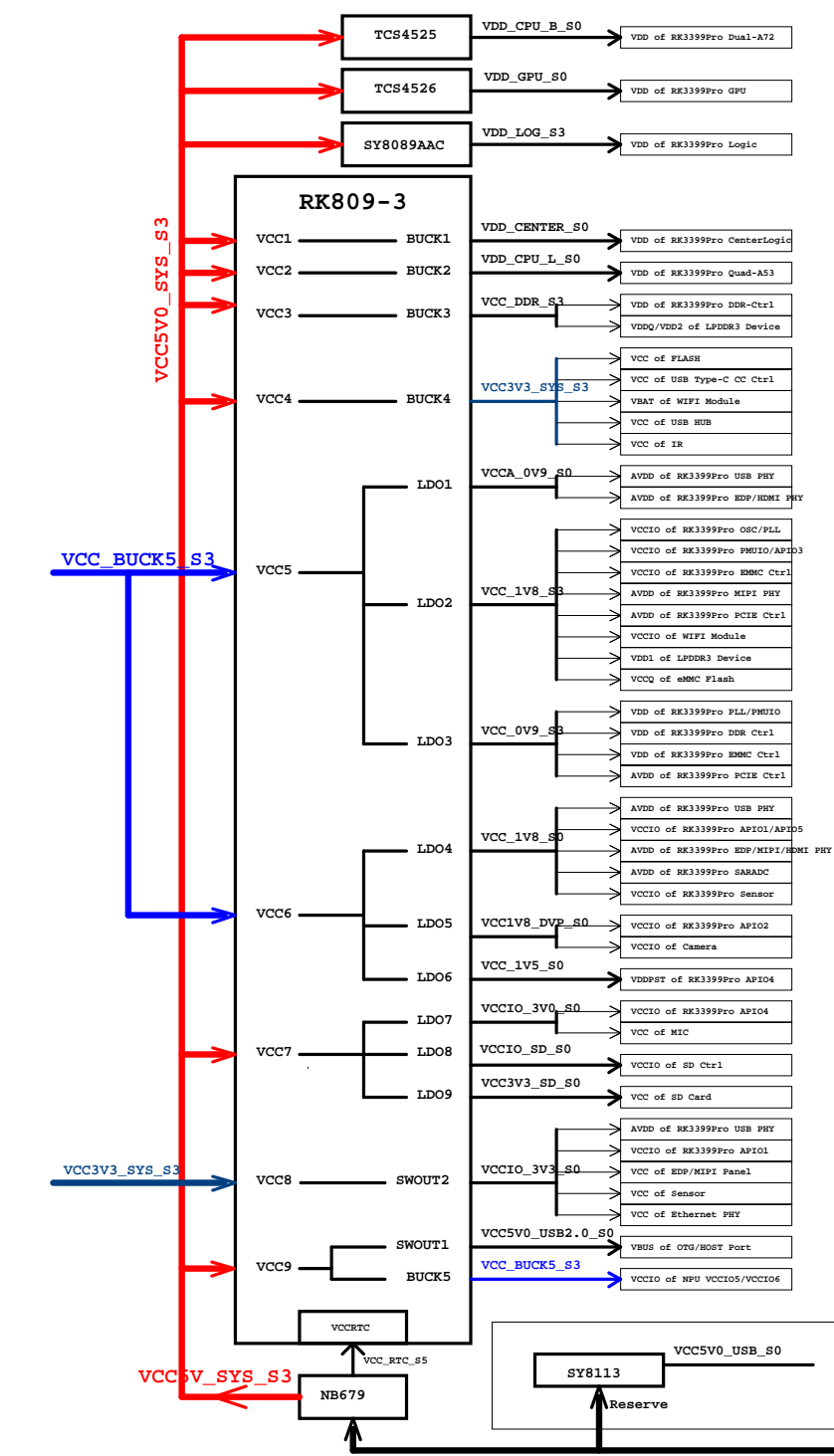
Rev:

V1.1

Sheet:

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Power Diagram and Sequence

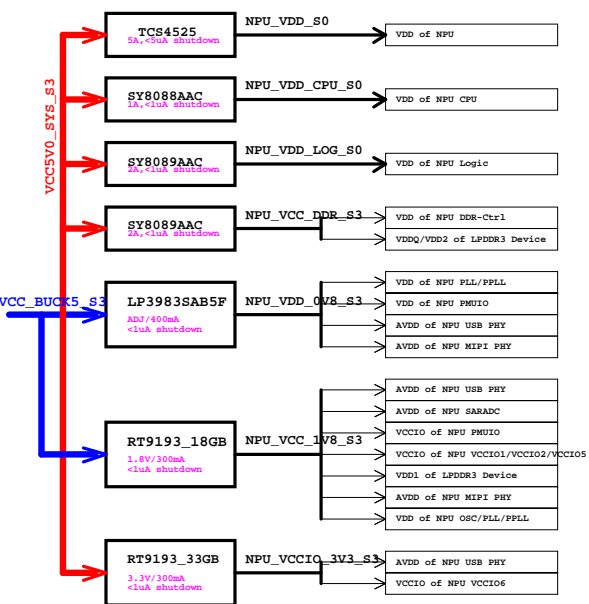


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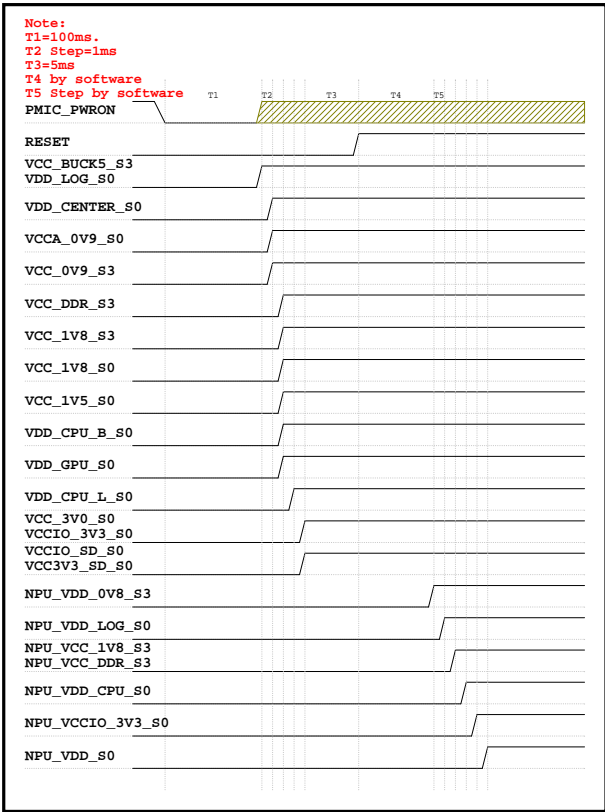
Notel:
Define of Power name's suffix:
S0: Keep on during working mode; Shut off during standby mode.
S3: Always on during working and standby mode.

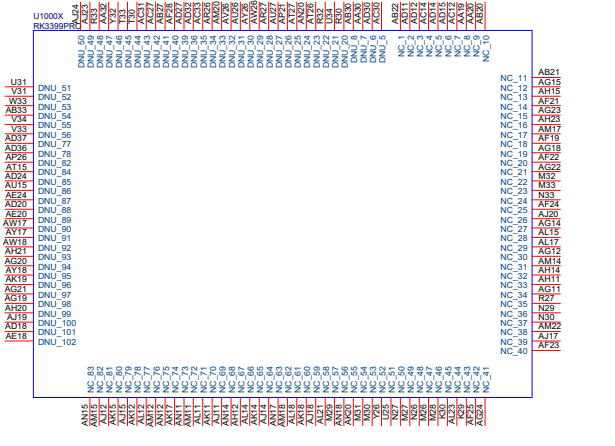
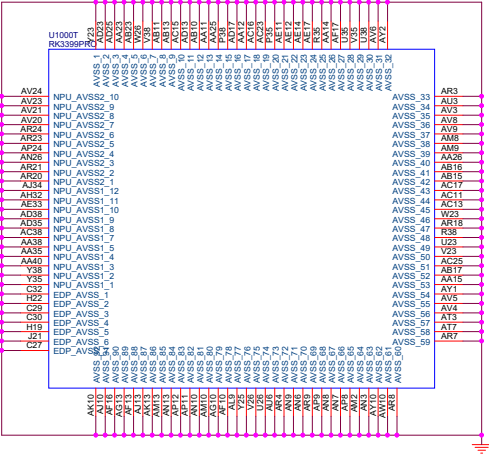
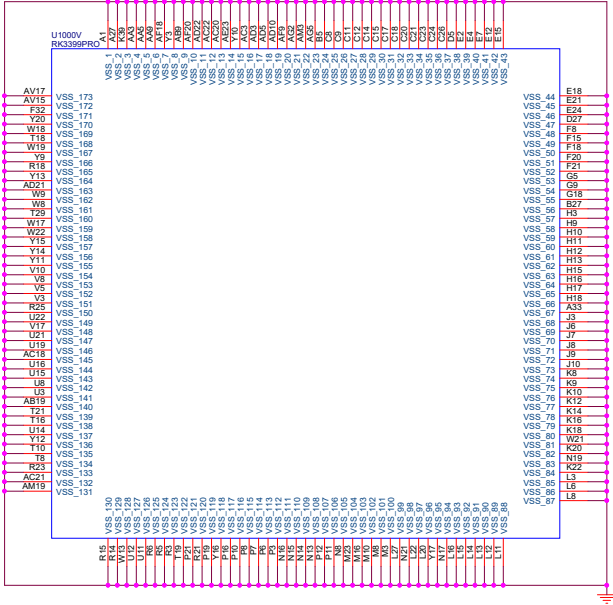
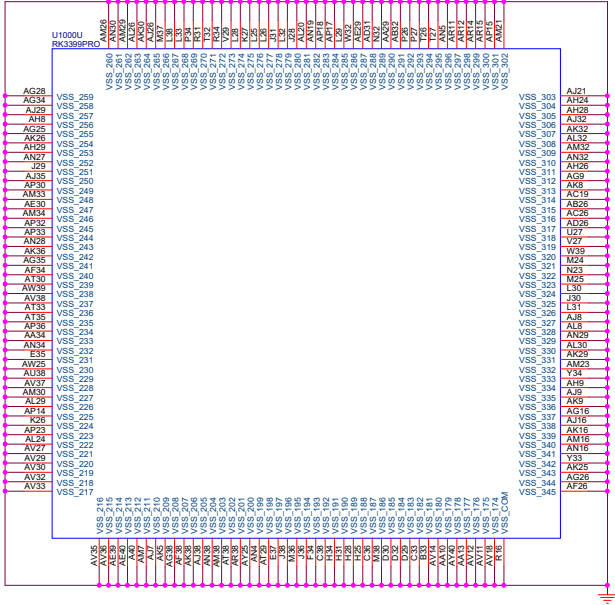
Note2:
"Peak current" shows Peak value of system consumption is normal work
and "Sleep current" is sleep mode.
"Peak current"指的是系统工作状态的峰值功耗数据，峰值数据，
"Sleep current" 是休眠状态峰值数据；

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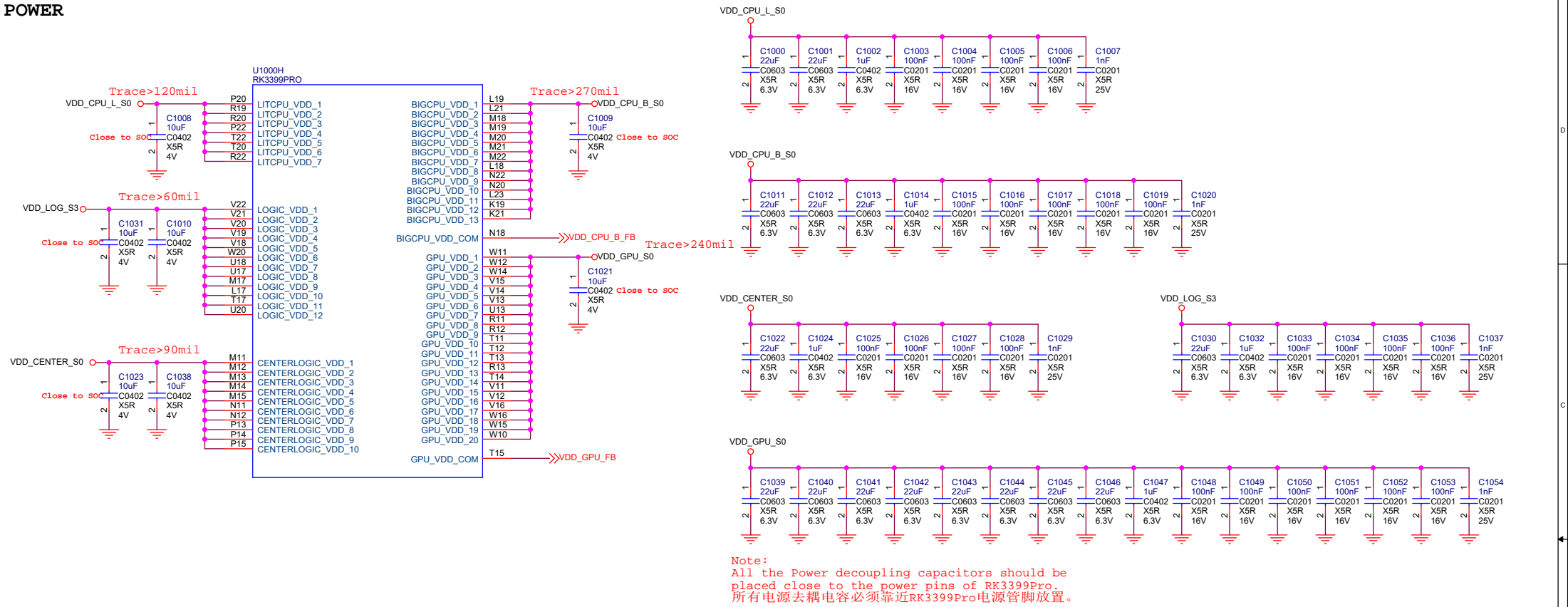


RK3399Pro Power-on Sequence									
Power Name	PMIC Channel	Time Slot (step 2ms)	Default voltage	Supply Limit	Default ON/OFF	sleep ON/OFF	Peak Current	sleep Current	
VCCVDD_SYS_S3	Ext:(NBW57)	Slot:0	5.0V	8.0A	ON	ON			
VCCVDD_SYS_S3	Ext:(NBW57)+B0CK3	Slot:1	3.3V	2.5A	ON	ON			
VDD_LOD_S3	Ext:(SY8089)	Slot:1A	0.9V	2.0A	ON	ON			
VDD_CENTRE_S3	Ext:(B0CK3)+B0CK3	Slot:2	0.9V	2.5A	ON	OFF			
VCC_VDD_S3	Ext:(B0CK3)+B0CK3	Slot:2	0.9V	0.4A	ON	OFF			
VCC_VDD_S3	Ext:(B0CK3)+L0CK3	Slot:2	0.9V	1.1A	ON	ON			
VCC_D0R_S3	Ext:(B0CK3)+B0CK3	Slot:3	1.25V	1.5A	ON	ON			
VCC_VDD_S3	Ext:(B0CK3)+L0CK3	Slot:3	1.8V	0.4A	ON	OFF			
VCC_V1B_S3	Ext:(B0CK3)+L0CK4	Slot:3	1.8V	0.4A	ON	OFF			
VCC_VDD_S3	Ext:(B0CK3)+L0CK6	Slot:3	1.5V	0.4A	ON	OFF			
VCC_VDD_B_S0	Ext:(T0C4525)	Slot:3A	0.9V	6.0A	ON	OFF			
VDD_GPD_S0	Ext:(T0C4526)	Slot:3B	0.9V	6.0A	ON	OFF			
VDD_CPU_L_S0	Ext:(B0CK3)+B0CK2	Slot:4	0.9V	2.5A	ON	OFF			
VCCVDD_V1B_S0	Ext:(B0CK3)+L0CK7	Slot:4	1.8V	0.4A	ON	OFF			
VCCVDD_V1B_S0	Ext:(B0CK3)+S0W072	Slot:5	3.3V	3.0A	ON	OFF			
VCCV1B_SYS_S3	Ext:(B0CK3)+B0CK4	Slot:5	3.3V	1.5A	ON	ON			
VCCVDD_B0_S0	Ext:(T0C4528)	Slot:5	3.3V	0.4A	ON	OFF			
VCCV1B_B0_S0	Ext:(B0CK3)+L0CK9	Slot:5	3.3V	0.4A	ON	OFF			
VCCV1B_DW_S0	Ext:(B0CK3)+L0CK5	Slot:6	1.8V	0.4A	OFF	OFF			
VCCV1B_DW_S0	Ext:(T0C4531)	Slot:6	1.5V	0.3A	OFF	OFF			
VCCVDD_WD_S0	Ext:(T0C4593)	Slot:7	2.8V	0.3A	OFF	OFF			
VCCVDD_WD_S0	Ext:(T0C4593)	Slot:7	1.5V	0.3A	OFF	OFF			
Ext:(NBW57)+B0CK3	Ext:(NBW57)+B0CK3	Slot:7	5.0V	1.5A	OFF	OFF			
Ext:(NBW57) sent out Reset signal for CPU(timing:10s); Then CPU sent out NPU's power-on signal									
NPD_VDD_OVB_S3	Ext:(IPI383)	Slot:11	0.8V	0.4A	ON	ON			
NPD_VDD_LOD_S3	Ext:(IPI383)+B0CK5	Slot:12	0.8V	2.0A	ON	ON			
NPD_VDD_V1B_S3	Ext:(T0C4593)	Slot:13	1.8V	0.3A	ON	ON			
NPD_VCC_D0R_S3	Ext:(SY8089)+B0CK5	Slot:13	1.25V	2.0A	ON	ON			
NPD_VDD_V1B_S3	Ext:(IPI383)+B0CK5	Slot:14	0.8V	0.4A	ON	ON			
NPD_VCCVDD_V1B_S3	Ext:(T0C4593)	Slot:15	3.3V	0.3A	ON	ON			
NPD_VDD_S0	Ext:(T0C4525)	Slot:16	0.85V	6.0A	ON	OFF			
CPU sent out LAM 0.8V for NPU									
CPU send out Reset signal for npu.									
NPU_RESET									

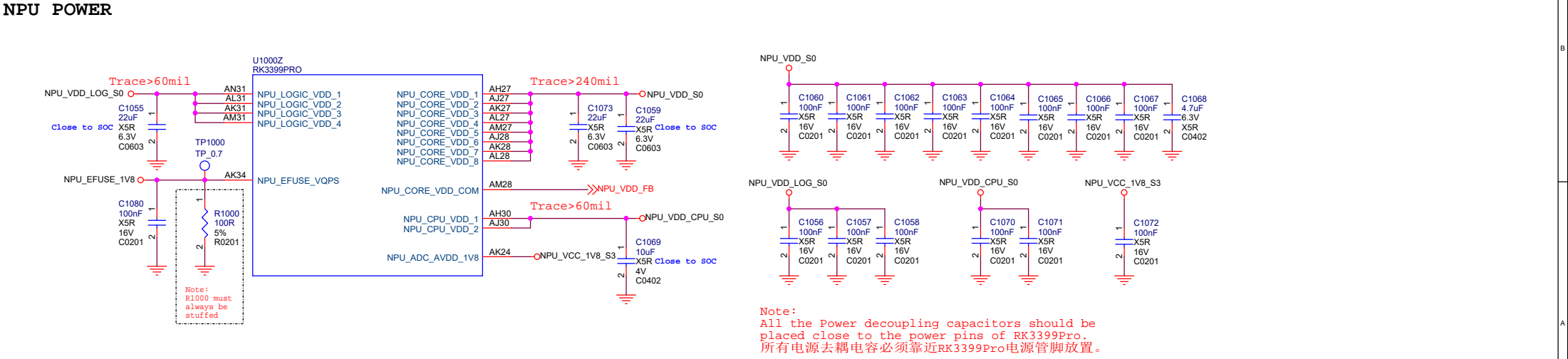




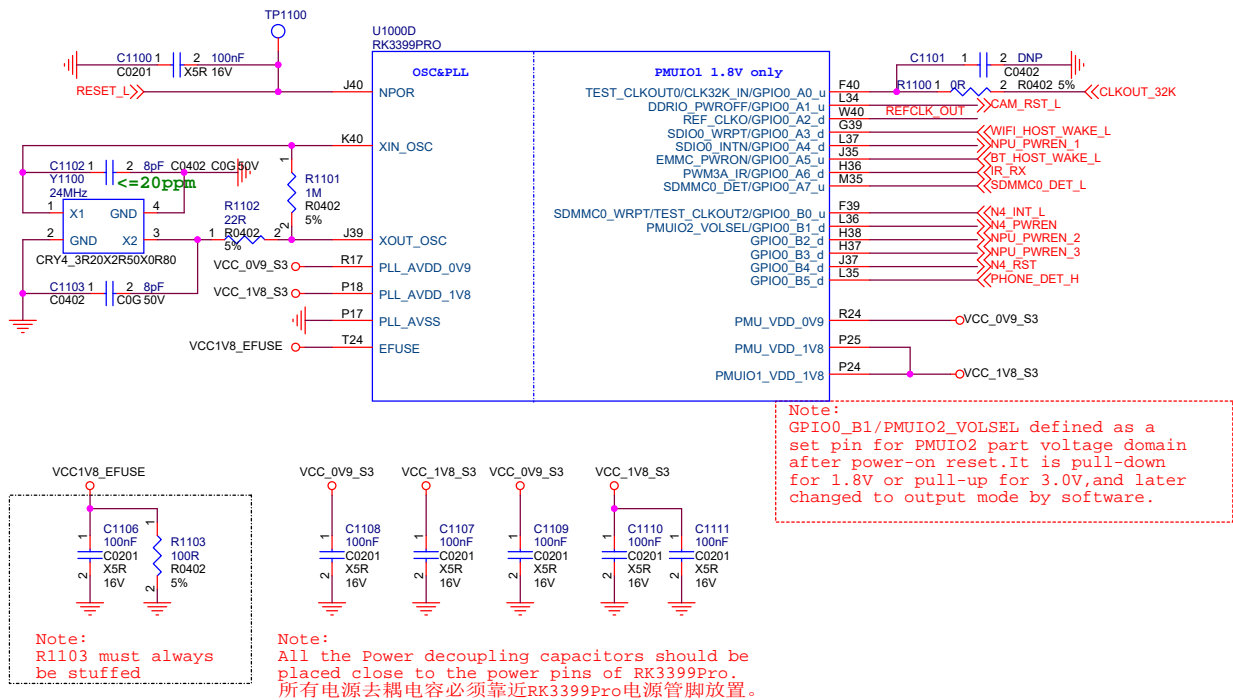
POWER



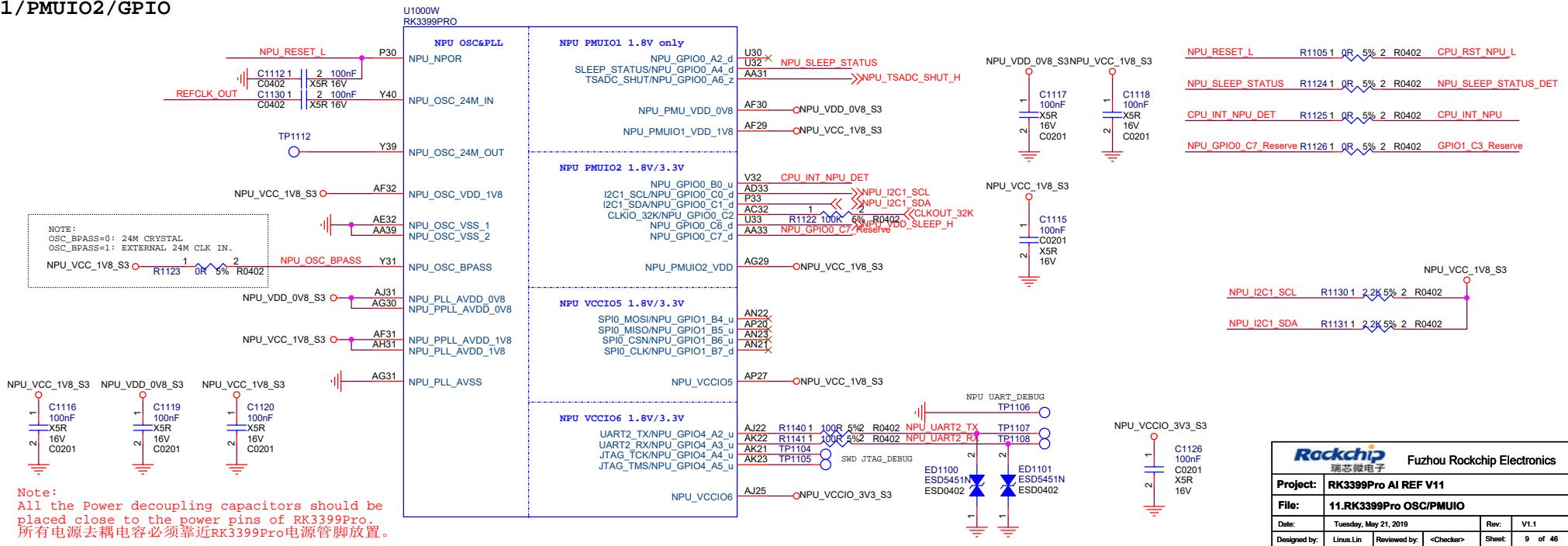
NPU POWER



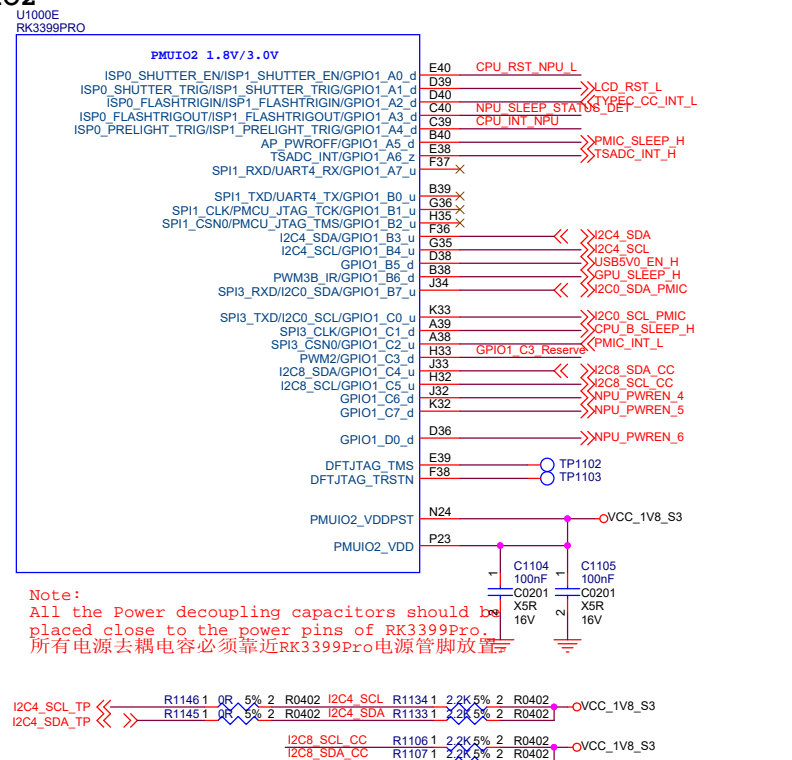
PMUIO1



NPU PMUIO1/PMUIO2/GPIO

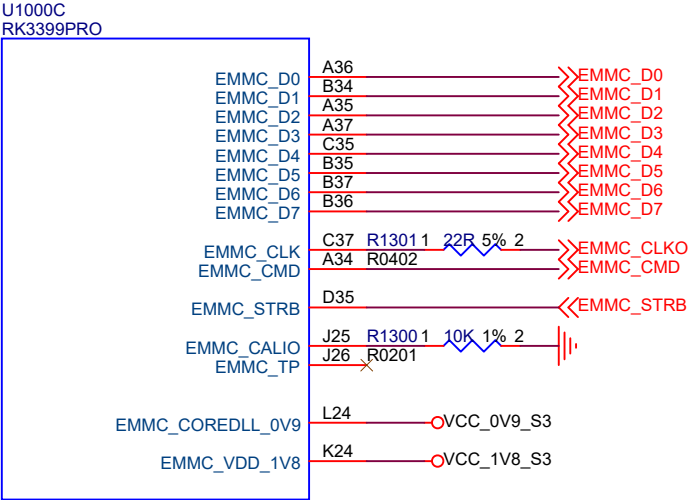


PMUIO2

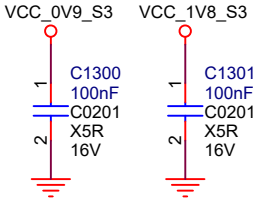


Rockchip 瑞芯微电子			
Fuzhou Rockchip Electronics			
Project:	RK3399Pro AI REF V11		
File:	11.RK3399Pro OSC/PMUIO		
Date:	Tuesday, May 21, 2019	Rev:	V1.1
Designed by:	Linus.Lin	Reviewed by:	<Checker>
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EMMC Controller



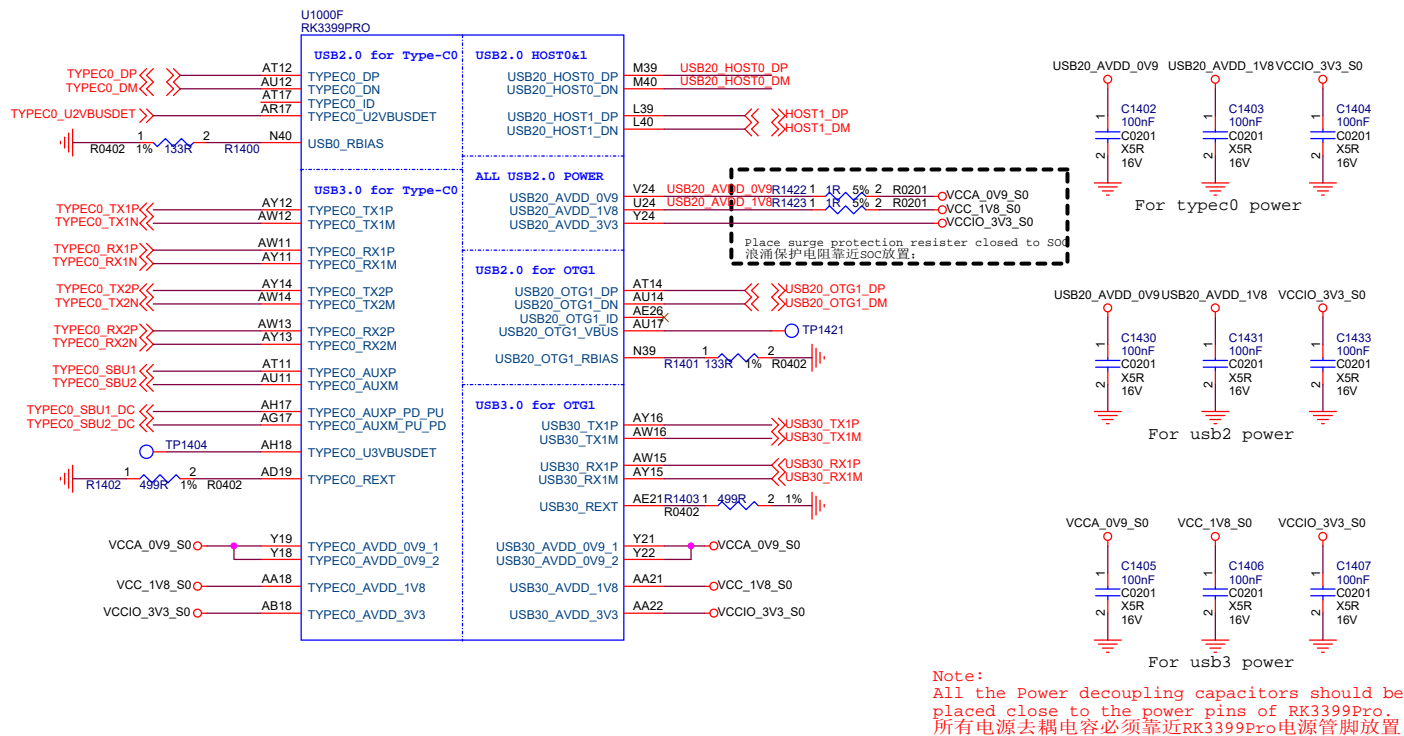
EMMC design rules:
1.Data[0:7],CMD and Strobe lines routing parallel as a group,and be isolated with other signals by GND line,the skew between group < 30ps;
2.Clk should be isolated with other signals by GND line;The skew between data signals < 20ps;
3.Max trace length < 3.93inchs;
4.Trace impedance 50ohm+/-10%;
5.The trace spacing with other signals follows the 3W rule;
6.R1300 should be place close to RK3399Pro;
EMMC信号设计规则:
1.Data[0:7]、CMD和Strobe整组并行走线并包地隔离;组内偏移小于200mil;
2.CLK单独包地走线,与数据信号的偏移小于20ps;
3.线长小于3.93英寸;
4.信号阻抗控制在50ohm+/-10%;
5.信号与其他信号的间距遵循3W原则;
6.R1300靠近RK3399Pro放置;



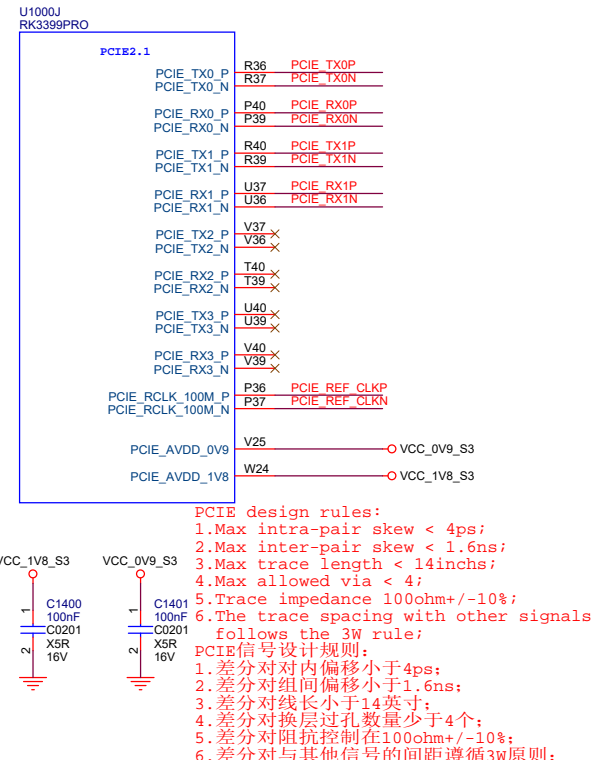
Note:
All the Power decoupling capacitors should be placed close to the power pins of RK3399Pro.
所有电源去耦电容必须靠近RK3399Pro电源管脚放置。

		Fuzhou Rockchip Electronics	
瑞芯微电子			
Project:	RK3399Pro AI REF V11		
File:	13.RK3399Pro EMMC Controller		
Date:	Tuesday, May 21, 2019		Rev: V1.1
Designed by:	Linus.Lin	Reviewed by: <Checker>	Sheet: 11 of 46

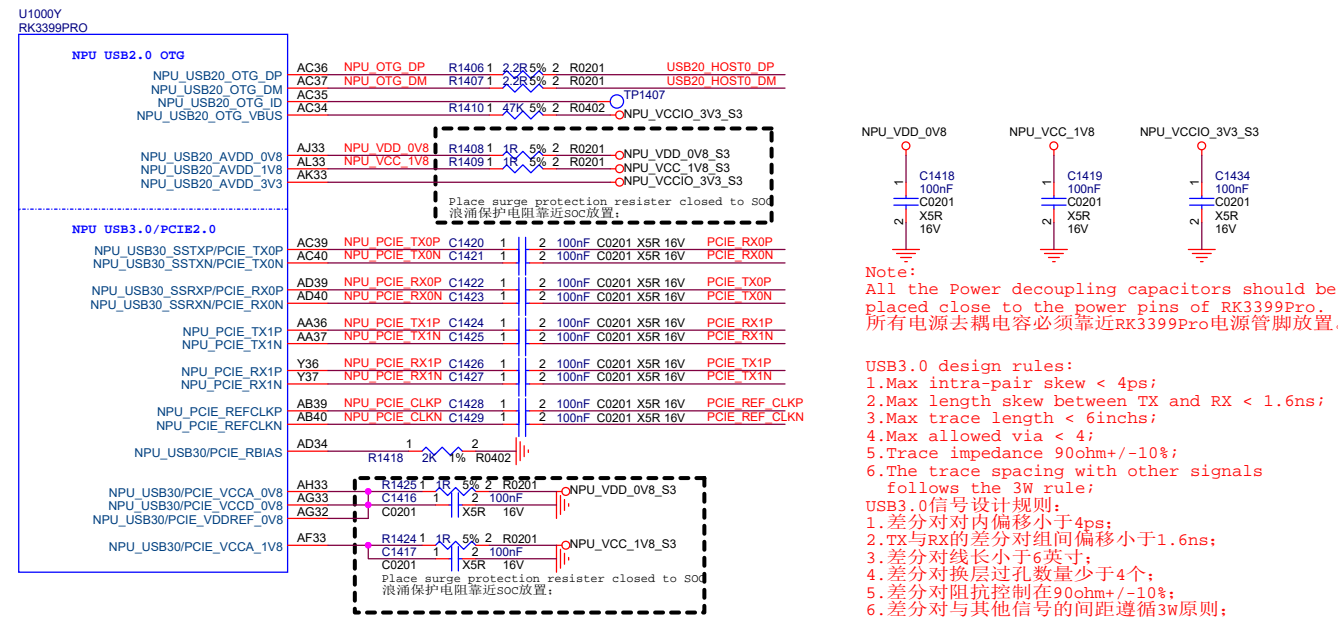
USB



PCIE



NPU PCIE/USB

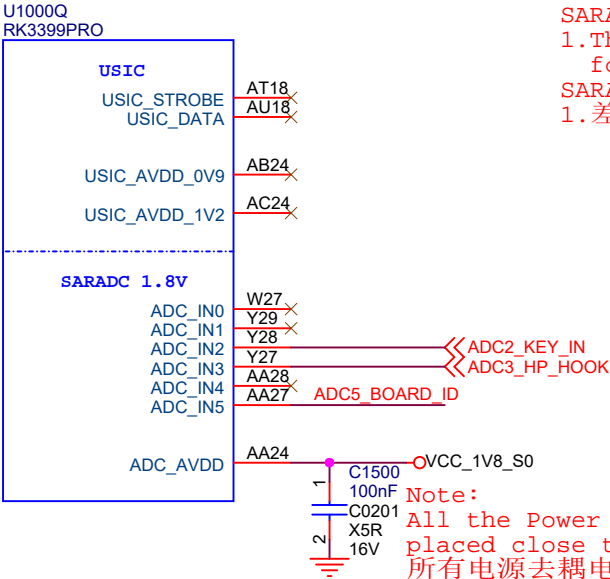


USB2.0 design rules:
1.Max intra-pair skew < 4ps;
2.Max trace length < 6inches;
3.Max allowed via < 6;
4.Trace impedance 90ohm+/-10%;
5.The trace spacing with other signals follows the 3W rule;
USB2.0信号设计规则:
1.差分对对内偏移小于4ps;
2.差分对线长小于6英寸;
3.差分对换层过孔数量少于6个;
4.差分对阻抗控制在90ohm+/-10%;
5.差分对与其他信号的间距遵循3W原则;

USB3.0 design rules:
1.Max intra-pair skew < 4ps;
2.Max length skew between TX and RX < 1.6ns;
3.Max trace length < 6inches;
4.Max allowed via < 4;
5.Trace impedance 90ohm+/-10%;
6.The trace spacing with other signals follows the 3W rule;
USB3.0信号设计规则:
1.差分对对内偏移小于4ps;
2.TX与RX的差分对组间偏移小于1.6ns;
3.差分对线长小于6英寸;
4.差分对换层过孔数量少于4个;
5.差分对阻抗控制在90ohm+/-10%;
6.差分对与其他信号的间距遵循3W原则;

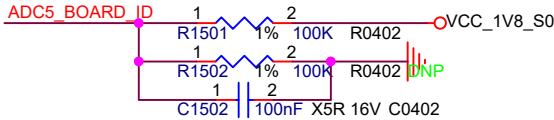
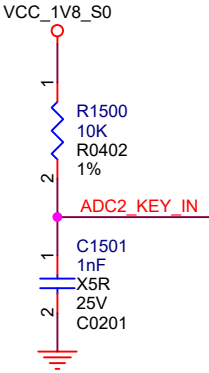
USIC&SARADC

Note:
Reserve ADC_IN2 for firmware update.If ADC2_KEY_IN=0V at power-on reset,then system will enter into Recovery/MiniLoader mode.
预留ADC_IN2用于固件升级，上电复位情况下如果ADC2_KEY_IN为低电平，系统会进入Recovery/MiniLoader模式。




SARADC design rules:
1.The trace spacing with other signals follows the 3W rule;
SARADC信号设计规则:
1.差分对与其他信号的间距遵循3w原则;

Note:
All the Power decoupling capacitors should be placed close to the power pins of RK3399Pro.
所有电源去耦电容必须靠近RK3399Pro电源管脚放置。



Vboard_id=1.8V, Version:V10;
Vboard_id=0.9V, Version:V20;
Vboard_id=0V, Version:V30;

 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399Pro AI REF V11		
File:	15.RK3399Pro SARADC/USIC		
Date:	Tuesday, May 21, 2019		Rev: V1.1
Designed by:	Linus.Lin	Reviewed by: <Checker>	Sheet: 13 of 46

VOP/CIF

U1000P
RK3399PRO

APIO2 1.8V/3.0V

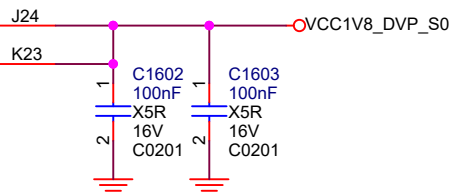
I2C2_SDA/VOP_D0/CIF_D0/GPIO2_A0_u
I2C2_SCL/VOP_D1/CIF_D1/GPIO2_A1_u
VOP_D2/CIF_D2/GPIO2_A2_d
VOP_D3/CIF_D3/GPIO2_A3_d
VOP_D4/CIF_D4/GPIO2_A4_d
VOP_D5/CIF_D5/GPIO2_A5_d
VOP_D6/CIF_D6/GPIO2_A6_d
I2C7_SDA/VOP_D7/CIF_D7/GPIO2_A7_u

D33 >> CIF_D0
J27 >> CIF_D1
F33 >> CIF_D2
E33 >> CIF_D3
G33 >> CIF_D4
G29 >> CIF_D5
H29 >> CIF_D6
G32 >> CIF_D7

I2C7_SCL/VOP_CLK/CIF_VSYNC/GPIO2_B0_u
I2C6_SDA/SPI2_RXD/CIF_HREF/GPIO2_B1_u
I2C6_SCL/SPI2_TXD/CIF_CLKIN/GPIO2_B2_u
SPI2_CLK/VOP_DEN/CIF_CLKOUTA/GPIO2_B3_u
SPI2_CSN0/GPIO2_B4_u

H30 >> CIF_VSYNC
G30 >> CIF_HREF
H26 >> CIF_CLKI
E34 >> CIF_CLK OUT
E32 >> DVP_PDN0_H

APIO2_VDDPST
APIO2_VDD



Note:
All the Power decoupling capacitors should be placed close to the power pins of RK3399Pro.
所有电源去耦电容必须靠近RK3399Pro电源管脚放置。

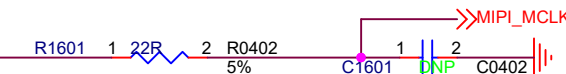
OPTION1

For cif camera, no used don't stuff



OPTION2

For mipi camera, No used don't stuff



NOTE:
R1600/R1601 Place on the same junction and close to RK3399Pro side.

NPU CIF

U1000M
RK3399PRO

NPU VCCIO2 1.8V/3.3V

NPU_CIF_D2/GPIO2_A4_d
NPU_CIF_D3/GPIO2_A5_d
NPU_CIF_D4/GPIO2_A6_d
NPU_CIF_D5/GPIO2_A7_d

W30 >> NPU_CIF_D2
V30 >> NPU_CIF_D3
P29 >> NPU_CIF_D4
Y30 >> NPU_CIF_D5

NPU_CIF_D6/GPIO2_B0_d
NPU_CIF_D7/GPIO2_B1_d
NPU_CIF_D8/GPIO2_B2_d
NPU_CIF_D9/GPIO2_B3_d
NPU_CIF_VSYNC/GPIO2_B4_d
NPU_CIF_HREF/GPIO2_B5_d
NPU_CIF_CLKIN_GPIO2_B6_d
NPU_CIF_CLKOUT/GPIO2_B7_d

AB29 >> NPU_CIF_D6
P28 >> NPU_CIF_D7
R29 >> NPU_CIF_D8
AD29 >> NPU_CIF_D9
AC29 >> NPU_CIF_VSYNC
U29 >> NPU_CIF_HREF
W29 >> NPU_CIF_CLKIN
U28 >> NPU_CIF_CLKOUT

NPU_CIF_D0/GPIO2_C0_d
NPU_CIF_D1/GPIO2_C1_d
NPU_CIF_D10/GPIO2_C2_d
NPU_CIF_D11/GPIO2_C3_d

R28 >> NPU_CIF_PDN0
AC28 >> NPU_CIF_PDN1
V28 >> NPU_CIF_RST
AD28 >> NPU_CIF_PWREN_H

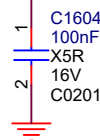
NPU_I2C3_SCL/GPIO2_D0_u
NPU_I2C3_SDA/GPIO2_D1_u

AF27 >> NPU_I2C3_SCL
AE27 >> NPU_I2C3_SDA

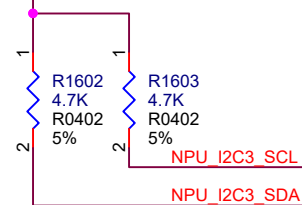
NPU_VCCIO2

AG27 >> NPU_VCC_1V8_S3

NPU_VCC_1V8_S3



NPU_VCC_1V8_S3



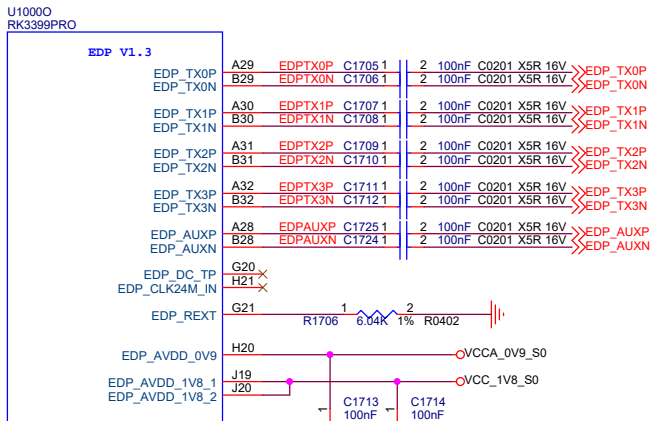
Note:
All the Power decoupling capacitors should be placed close to the power pins of RK3399Pro.
所有电源去耦电容必须靠近RK3399Pro电源管脚放置。

Rockchip
瑞芯微电子


Fuzhou Rockchip Electronics

Project:	RK3399Pro AI REF V11		
File:	16.RK3399Pro VOP/CIF		
Date:	Tuesday, May 21, 2019	Rev:	V1.1
Designed by:	Linus.Lin	Reviewed by:	<Checker>
Sheet:	14 of 46		

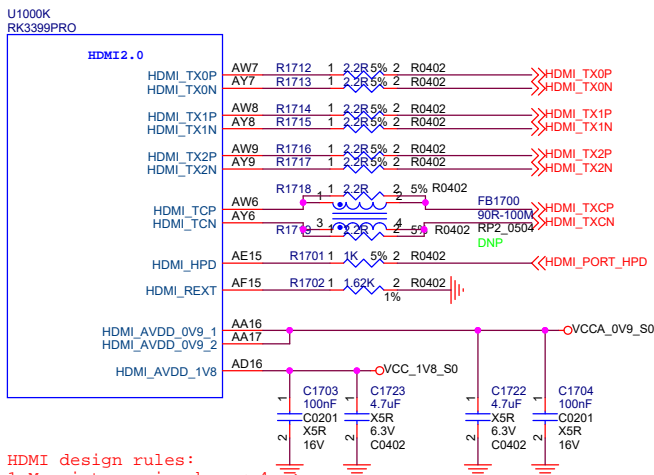
EDP



eDP design rules:

- | | |
|--|---|
| 1.Max intra-pair skew <4 ps;
2.Max trace length < 6inches;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The trace spacing with other signals follows the 3W rule; | 
Note:
All the Power decoupling capacitors should be placed close to the power pins of RK3399Pro.
所有电源去耦电容必须靠近RK3399Pro 电源管脚放置。 |
|--|---|
- eDP信号设计规则:
- 1.差分对对内偏移小于4ps;
 - 2.差分对线长小于6英寸;
 - 3.差分对换层过孔数量少于4个;
 - 4.差分对阻抗控制在90ohm+/-10%;
 - 5.差分对与其他信号的间距遵循3W原则;

HDMI



HDMI design rules:

1. Max intra-pair skew < 4ps;
2. Max length skew between clk and data < 80ps;
3. Max trace length < 9.8inches;
4. Max allowed via < 4;
5. Trace impedance 100ohm+/-10%;
6. The trace spacing with other signals follows the 3W rule;

HDMI信号设计规则:

1. 差分对对内偏移小于4ps;
2. Clk与Data的差分对组间偏移小于80ps;
3. 差分对线长小于9.8英寸;
4. 差分对换层过孔数量少于4个;
5. 差分对阻抗控制在100ohm+/-10%;
6. 差分对与其他信号的间距遵循3W原则;

MIPI CSI/DSI



Note:

All the Power decoupling capacitors should be placed close to the power pins of RK3399Pro.
所有电源去耦电容必须靠近RK3399Pro电源管脚放置。

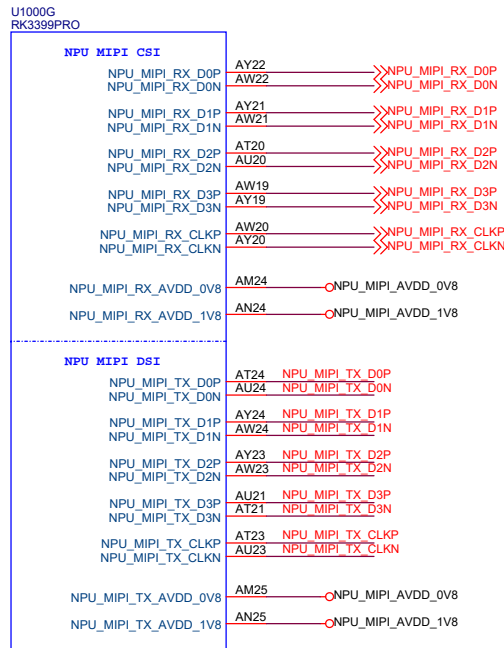
MIPI design rules:

- 1.Max intra-pair skew < 4ps;
- 2.Max length skew between clk and data < 7ps;
- 3.Max trace length < 7.2inches;
- 4.Max allowed via < 4;
- 5.Trace impedance 100ohm+/-10%;
- 6.The trace spacing with other signals follows the 3W rule;

MIPI信号设计规则:

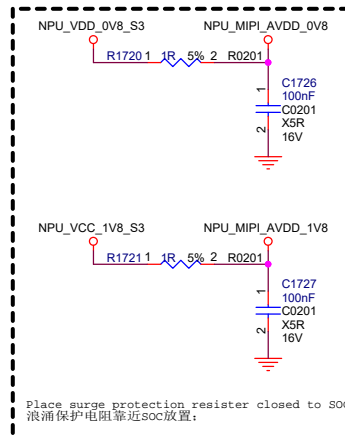
1. 差分对对内偏移小于4ps;
2. Clk与Data的差分对组间偏移小于7ps;
3. 差分对线长小于7.2英寸;
4. 差分对换层过孔数量少于4个;
5. 差分对阻抗控制在100ohm+/-10%;
6. 差分对与其他信号的间距遵循3w原则;

NPU MIPI CSI/DSI

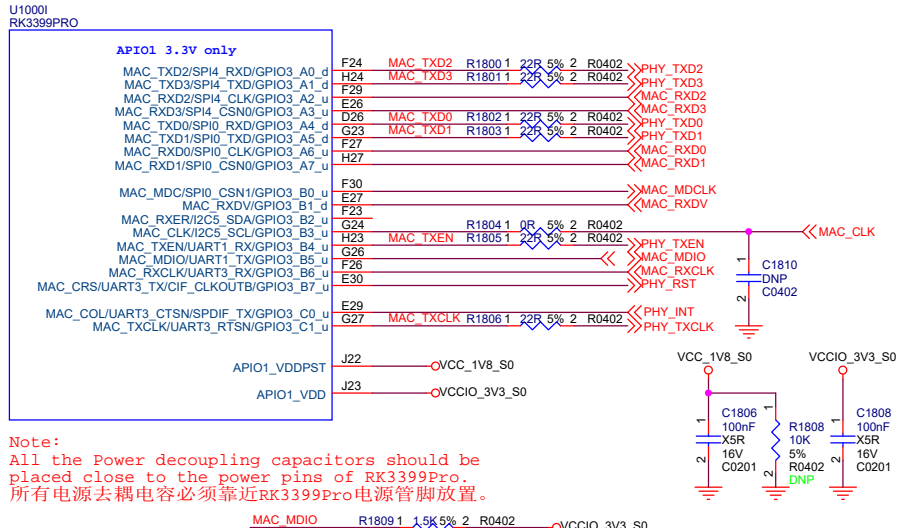


Note:

All the Power decoupling capacitors should be placed close to the power pins of RK3399Pro.
所有电源去耦电容必须靠近RK3399Pro电源管脚放置。

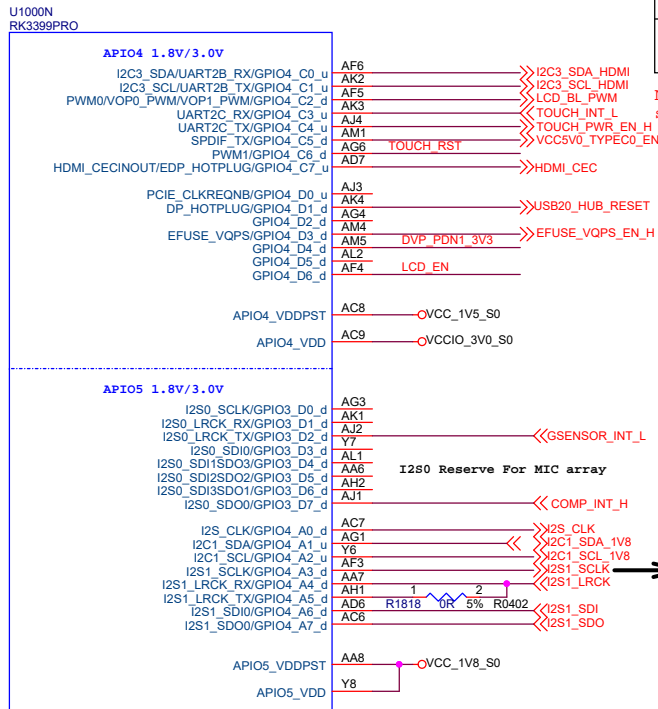


APIO1



Note:
All the Power decoupling capacitors should be placed close to the power pins of RK3399Pro.
所有电源去耦电容必须靠近RK3399Pro电源管脚放置。

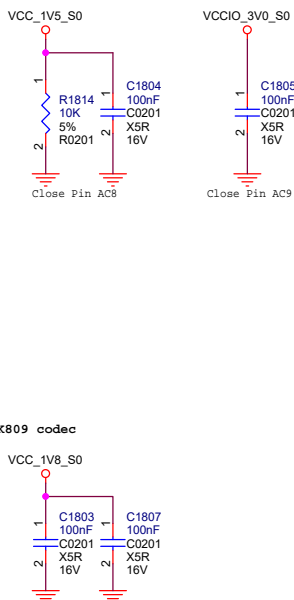
API04 / API05



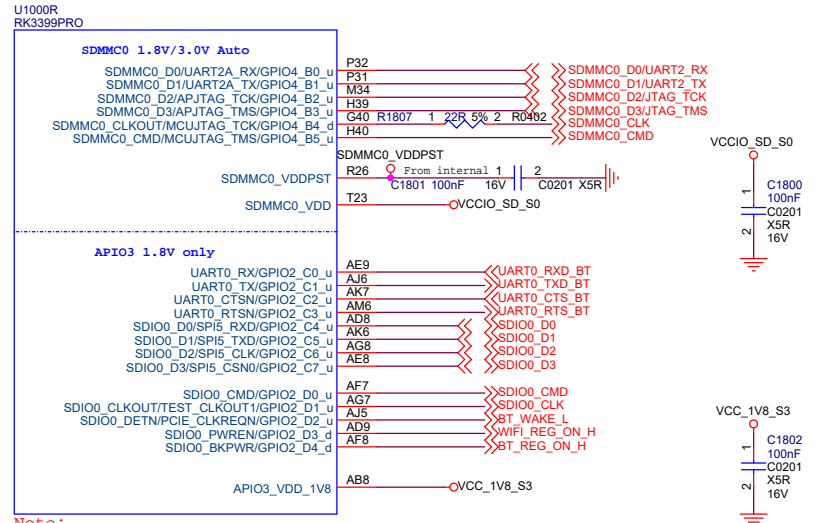
Note:
All the Power decoupling capacitors should be placed close to the power pins of RK3399Pro.
所有电源去耦电容必须靠近RK3399Pro电源管脚放置。

1.8V Only	VDDPST=VDDIO=1.8V
3.3V Only	VDDPST=1.8V, VDDIO=3.3V
1.8V/3.0V mode	3.0V mode: VDDPST=1.5V, VDDIO=3.0V 1.8V mode: VDDPST=1.8V, VDDIO=1.8V

Note: All the part which support 1.8V and 3.0V mode, software config should match with hardware design.



SDMMC0 / APIO3



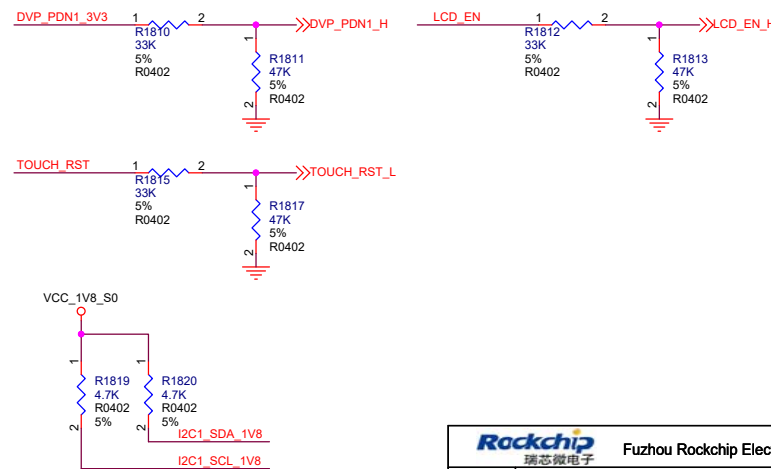
Note:
All the Power decoupling capacitors should be placed close to the power pins of RK3399Pro.
所有电源去耦电容必须靠近RK3399Pro电源管脚放置。

SDMMC/SDIO design rules:

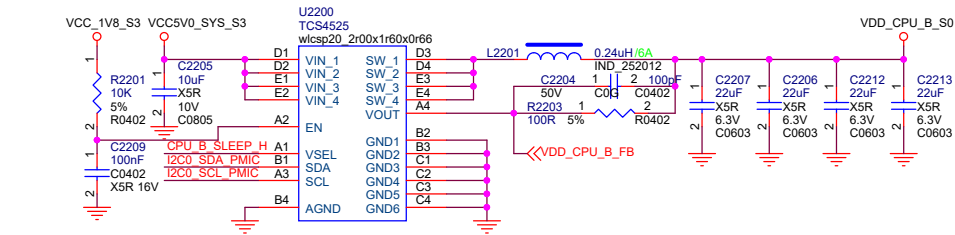
- 1.Data[0:3] and CMD lines routing parallel as a group,and be isolated with other signals by GND line,the skew between group < 30ps;
- 2.CLK should be isolated with other signals by GND line;The skew between data signals < 20ps;
- 3.Max trace length < 3.93inches;
- 4.Trace impedance 50ohm+/-10%;
- 5.The trace spacing with other signals follows the 3W rule;

SDMMC/SDIO信号设计规则:

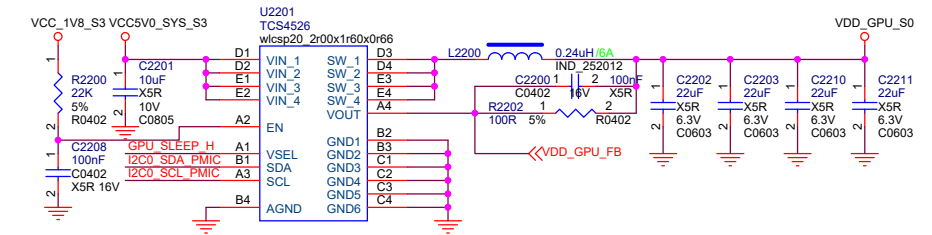
- 1.Data[0:3]和CMD整组并行走线并包地隔离;组内偏移小于200mil;
- 2.CLK单独包地走线,与数据信号的偏移小于20ps;
- 3.线长小于3.93英寸;
- 4.信号阻抗控制在50ohm+/-10%;
- 5.信号与其他信号的间距遵循3W原则;



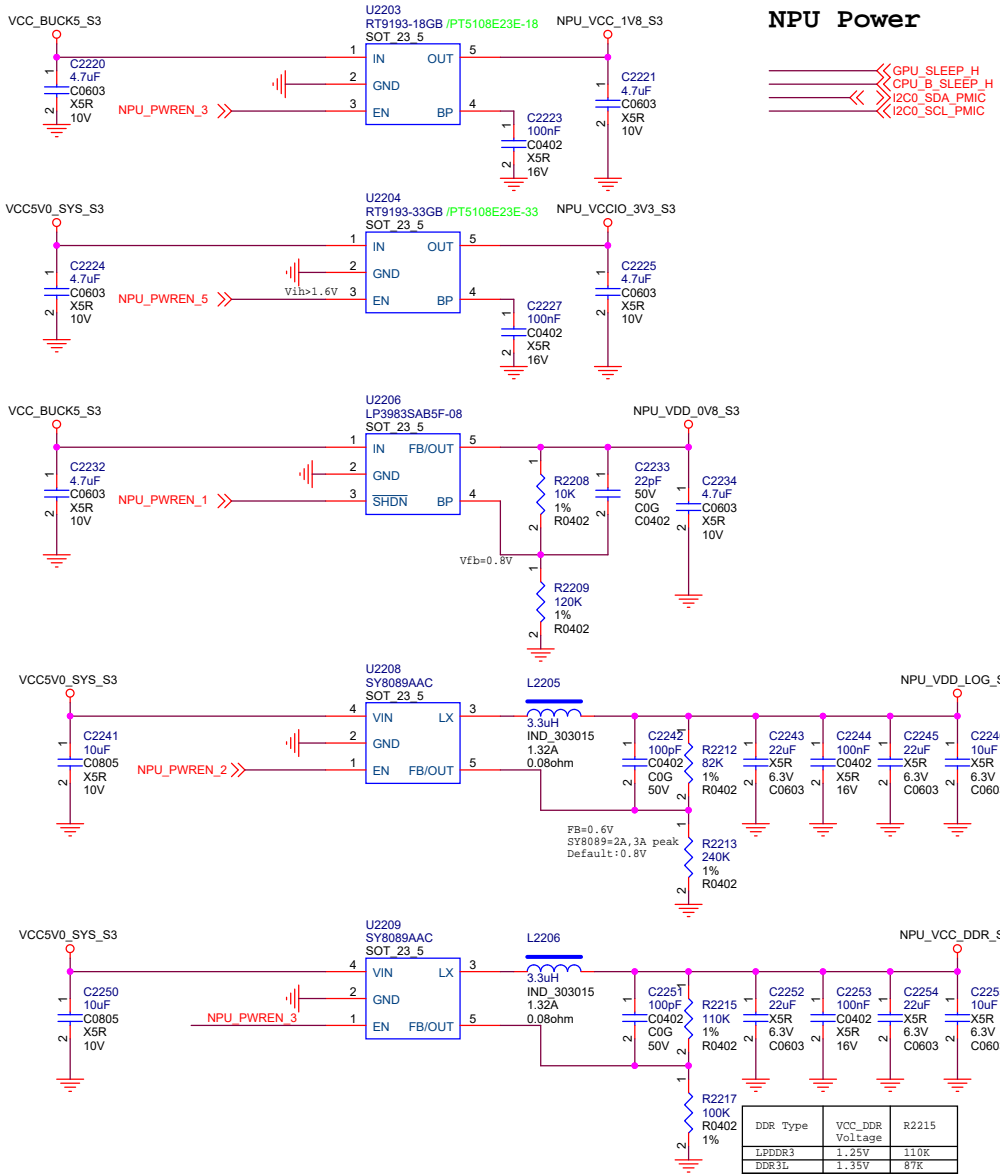
VDD_CPU_B power



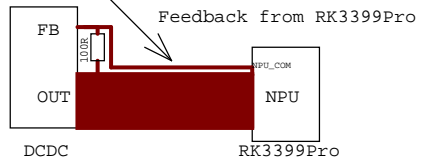
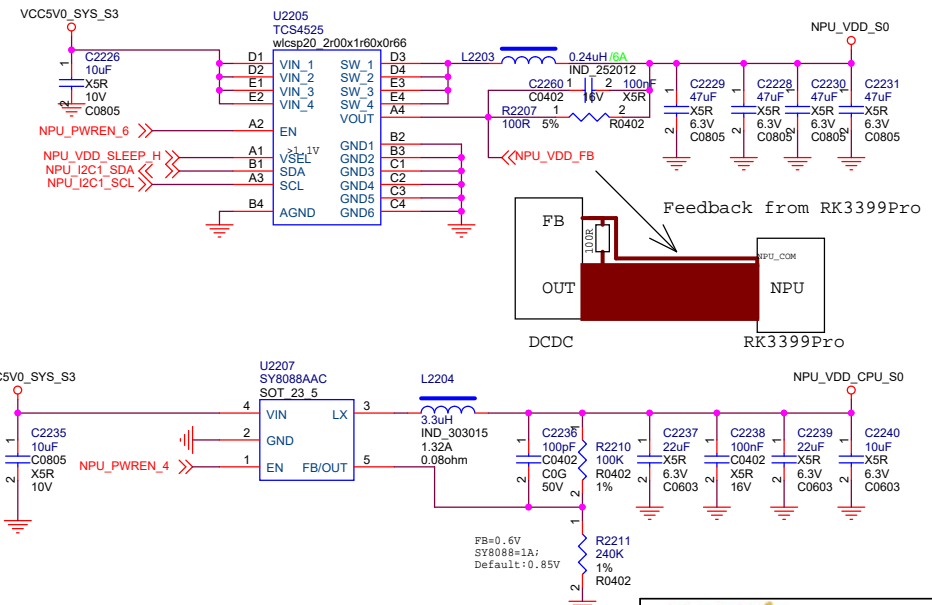
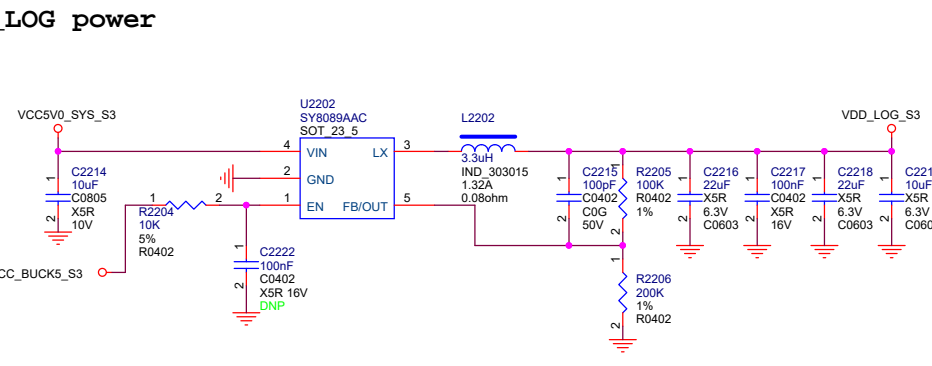
VDD_GPU power



NPU Power



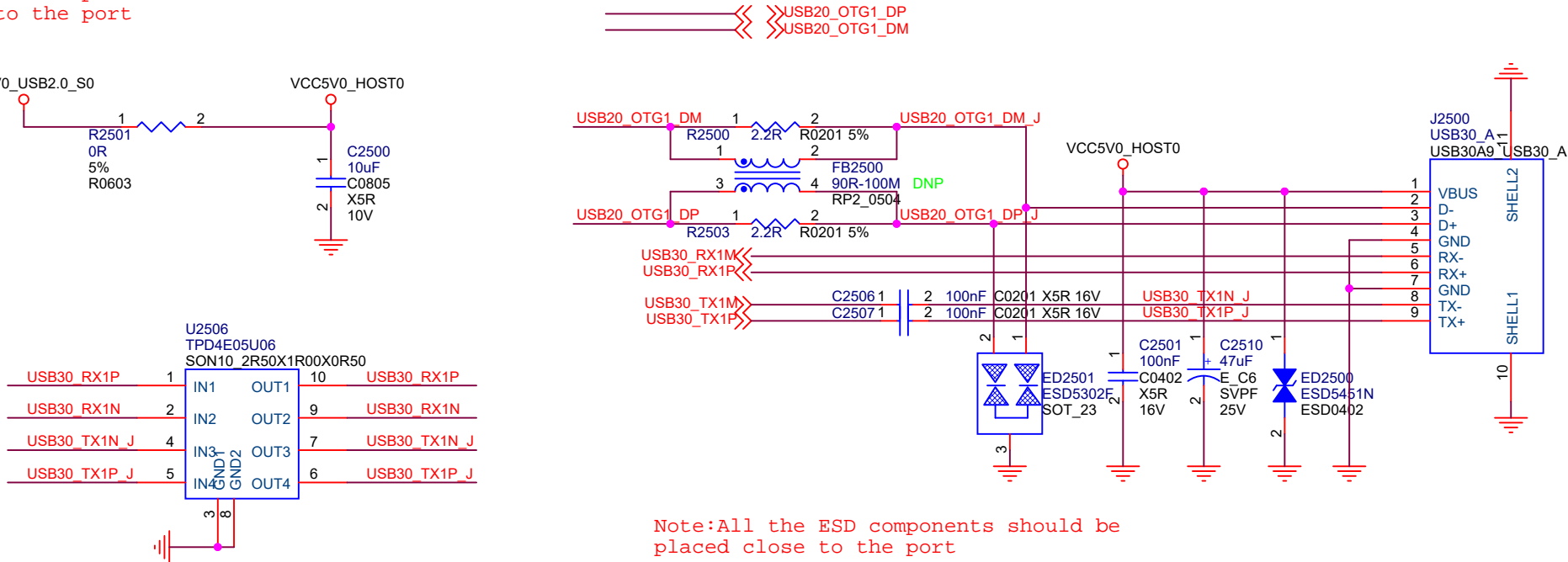
VDD_LOG power



DDR Type	VCC_DDR Voltage	R2215
LPDDR3	1.25V	110K
DDR3L	1.35V	87K

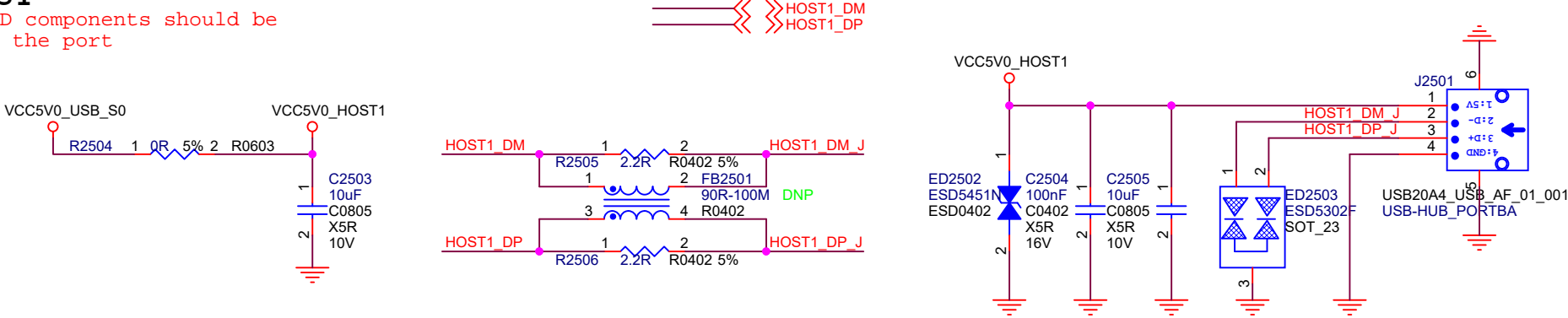
USB3.0 HOST

Note:All the ESD components should be placed close to the port

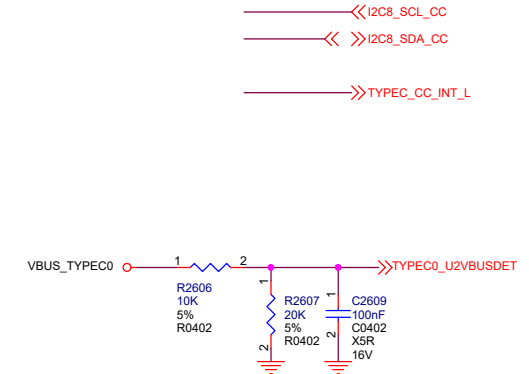
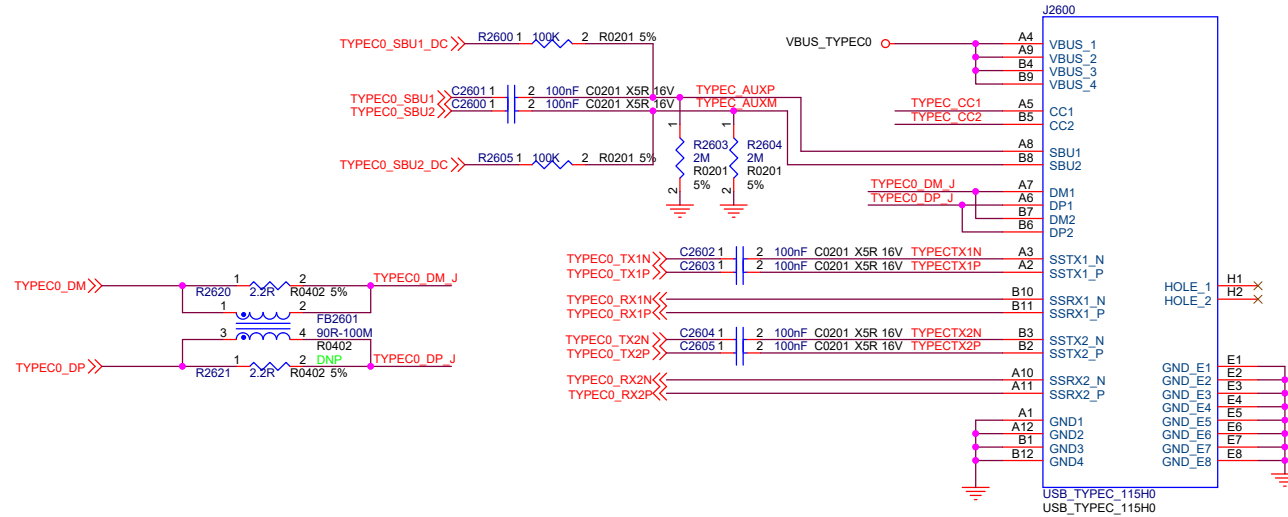


USB2.0 HOST

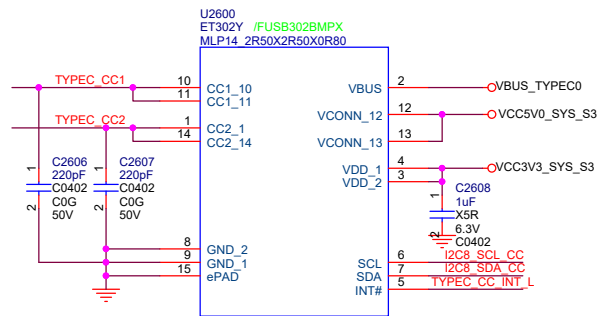
Note:All the ESD components should be placed close to the port



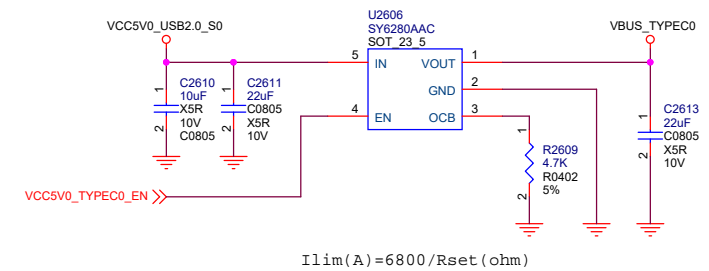
USB Detection



USB Type-C CC Ctrl

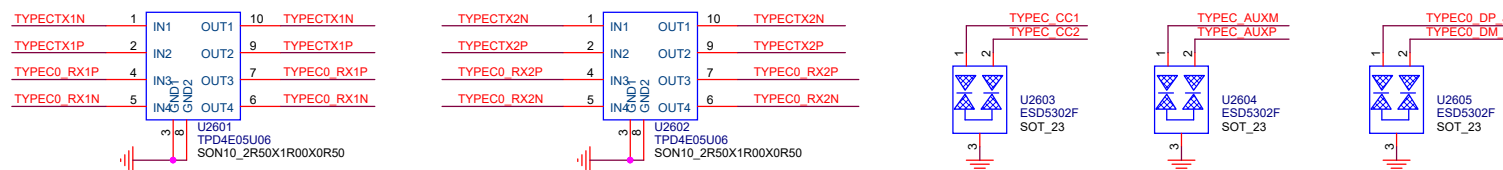


USB Type-C Power

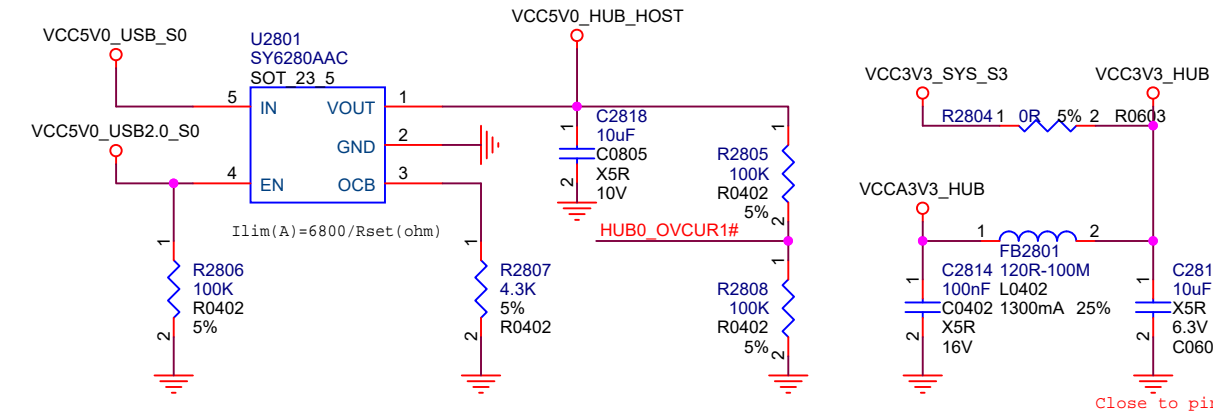
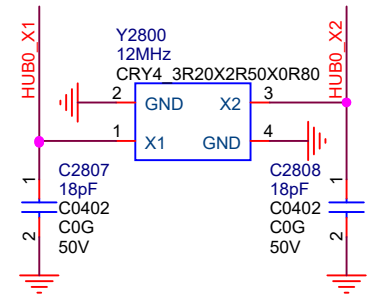
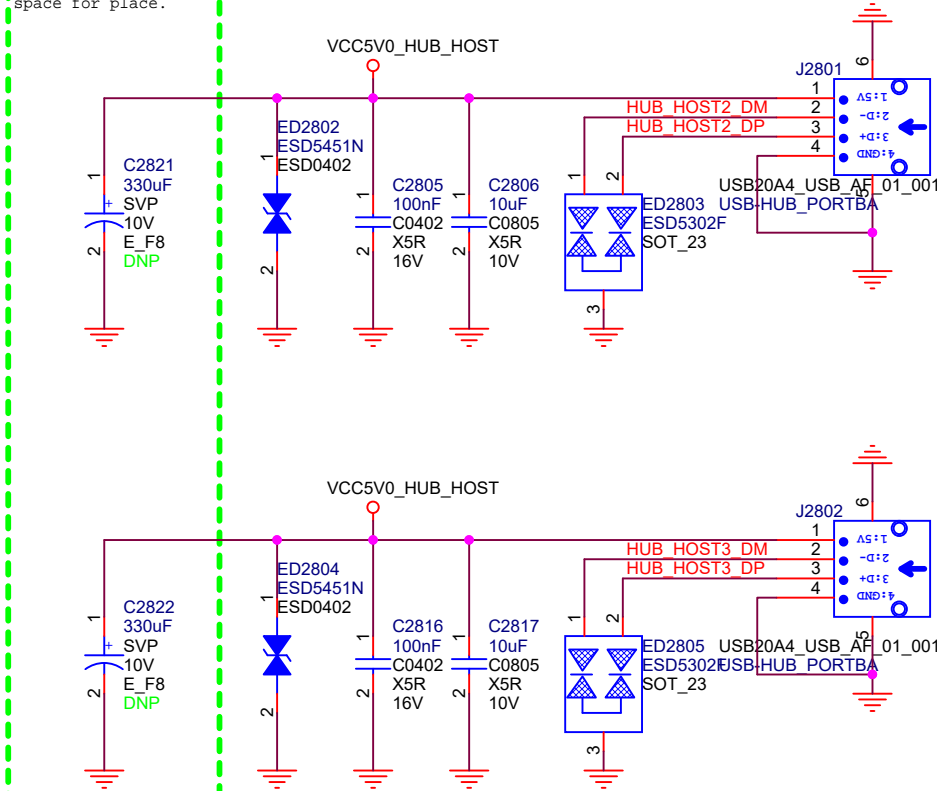
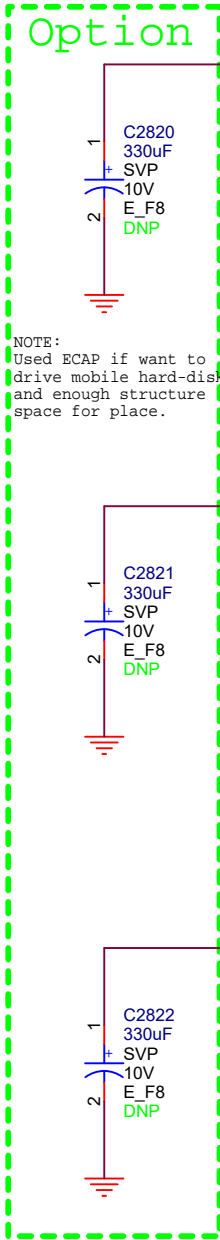
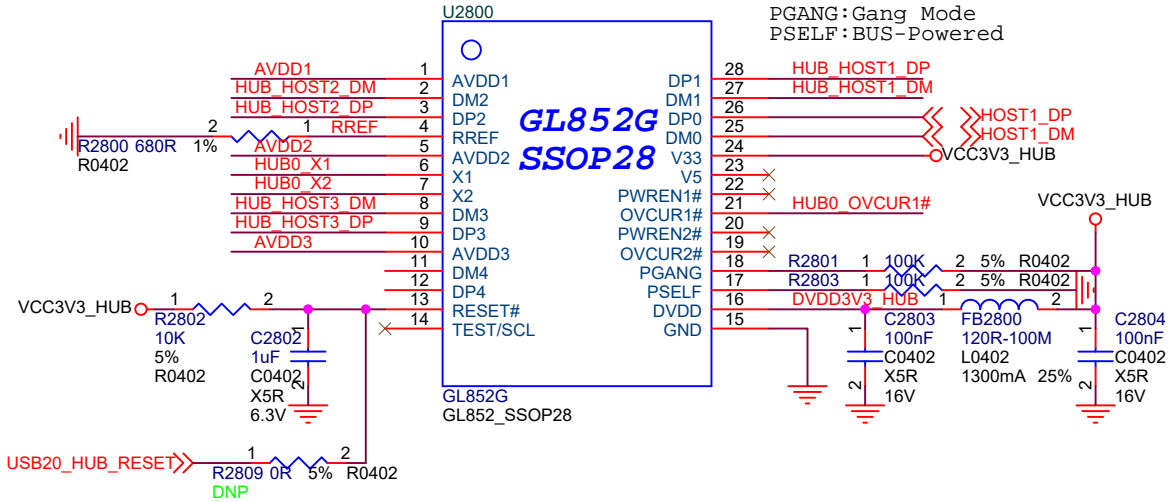



ESD

Note: All the ESD components should be placed close to the port and $C_j \leq 0.4 \text{ pF}$



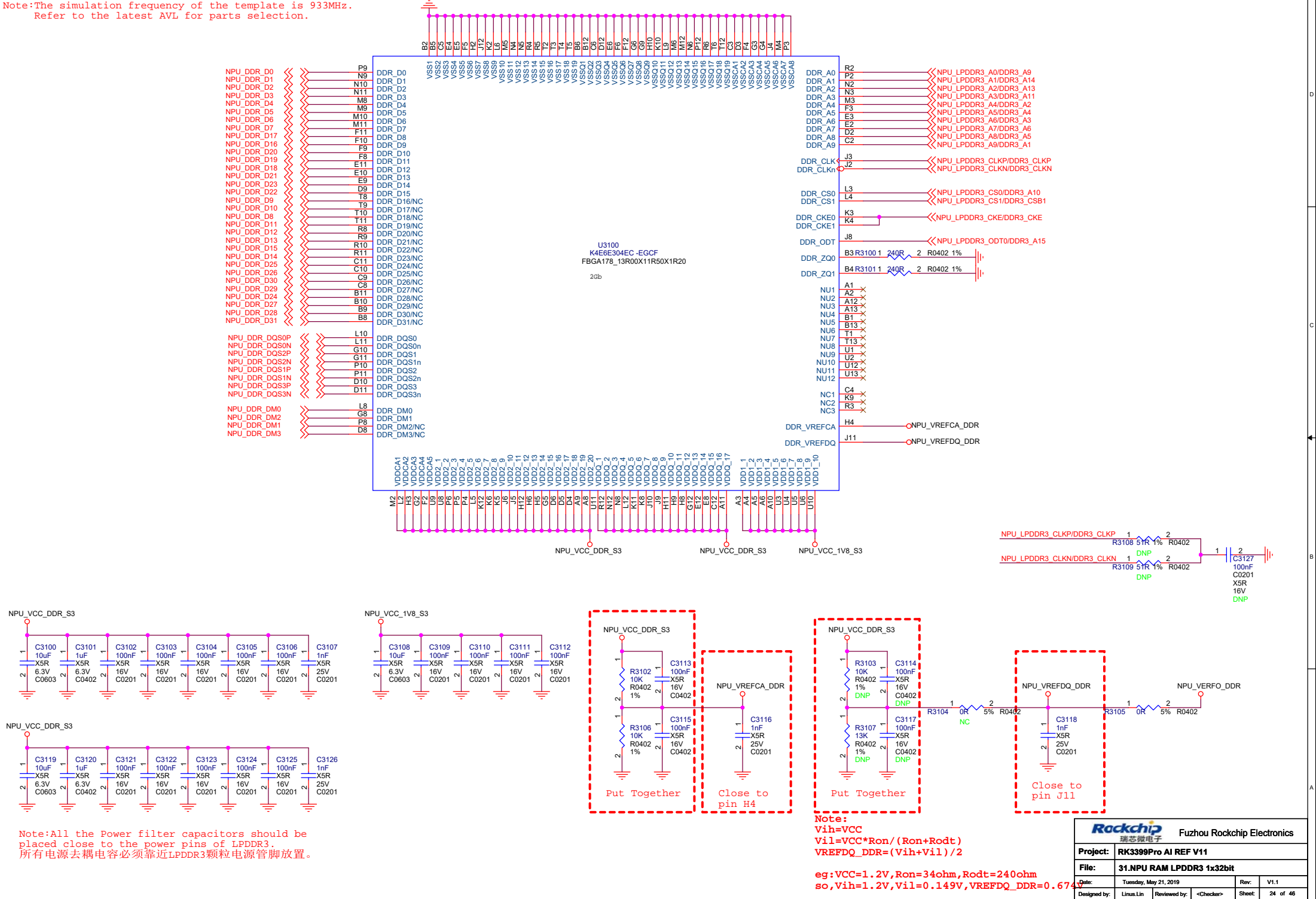
USB2.0 HUB



 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399Pro AI REF V11		
File:	28.USB HUB GL85x (option)		
Date:	Tuesday, May 21, 2019		Rev: V1.1
Designed by:	Linus.Lin	Reviewed by: <Checker>	Sheet: 22 of 46

NPU LPDDR3 1x32bit

Note:The simulation frequency of the template is 933MHz.
Refer to the latest AVL for parts selection.

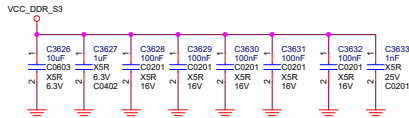
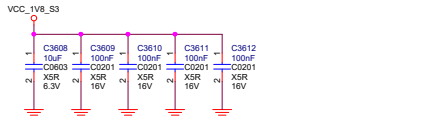
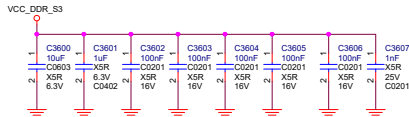
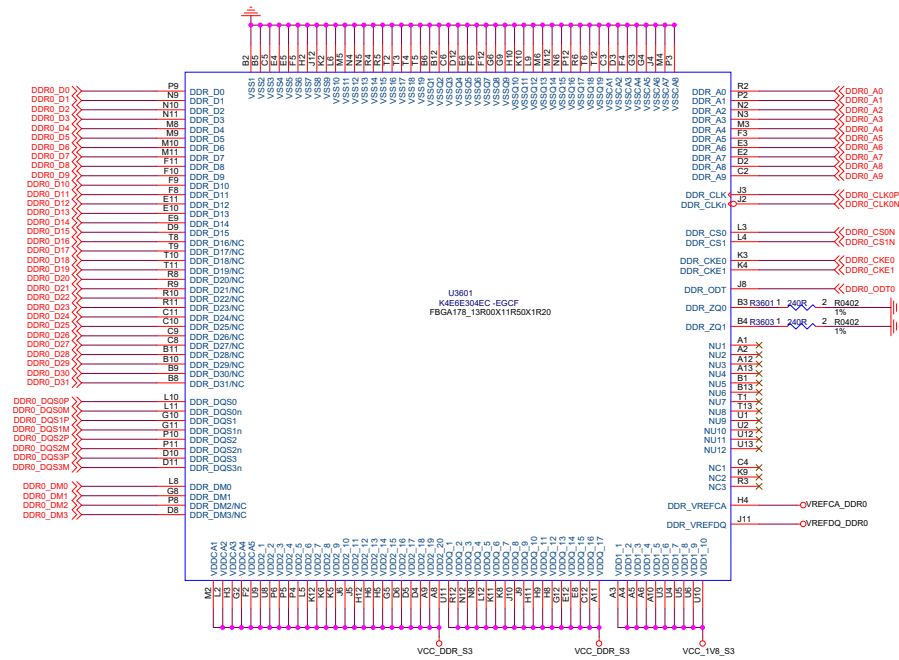
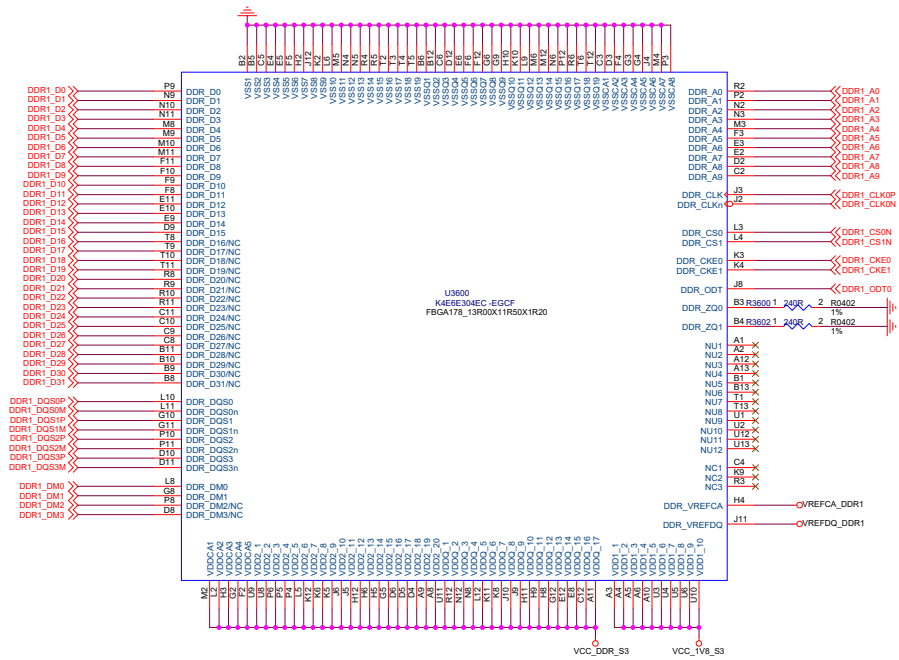




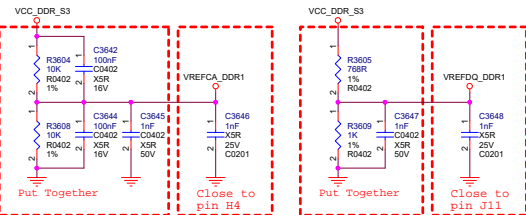
LPDDR3 2x32bit 178A11

Note:The simulation frequency of the template is 933MHz.

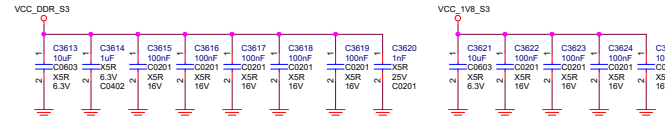
Refer to the latest AVL for parts selection.



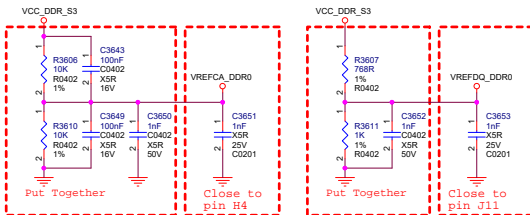
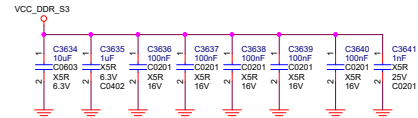
Note:All the Power filter capacitors should be placed close to the power pins of LPDDR3.
所有电源去耦电容必须靠近LPDDR3颗粒电源管脚放置。



Note:
Vih=VCC
Vil=VCC*Ron/(Ron+R0dt)
VREFDQ_DDR=(Vih+Vil)/2
eg:VCC=1.2V,Ron=34ohm,R0dt=240ohm
so,Vih=1.2V,Vil=0.149V,VREFDQ_DDR=0.674V



Note:All the Power filter capacitors should be placed close to the power pins of LPDDR3.
所有电源去耦电容必须靠近LPDDR3颗粒电源管脚放置。



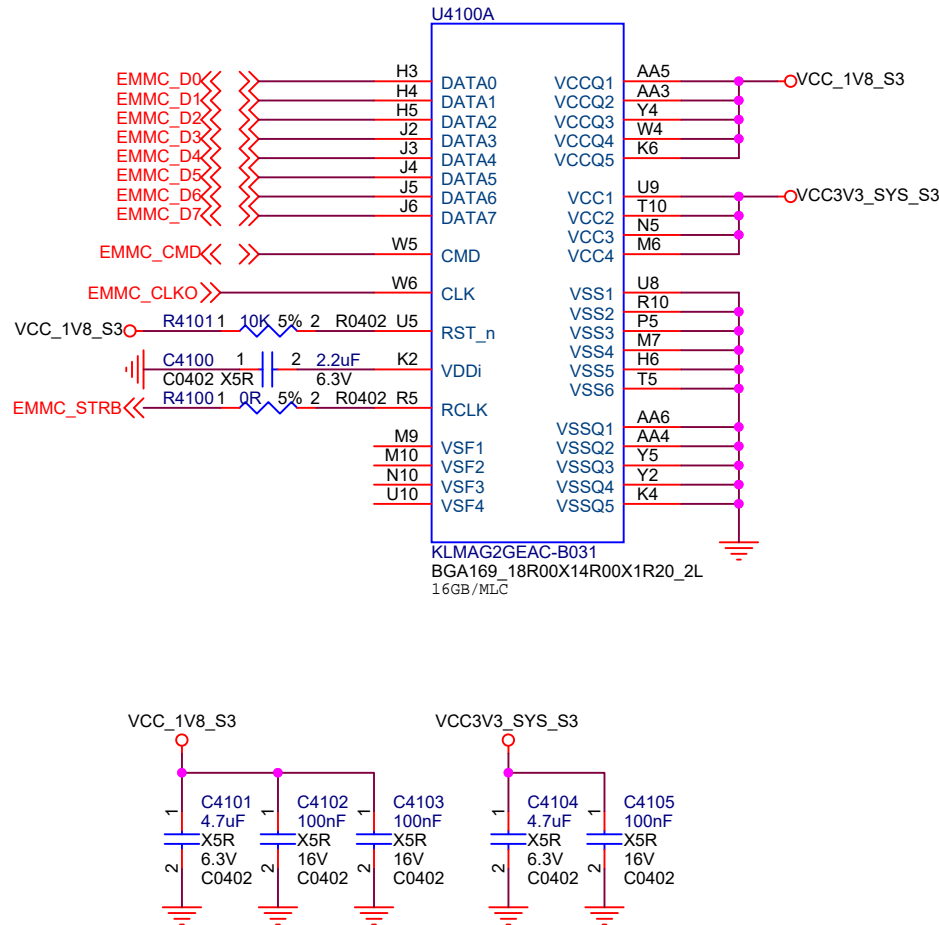
CPU LPDDR4

Note: The simulation frequency of the template is 800MHz.
Refer to the latest AVL for parts selection.
All the data can't be swap

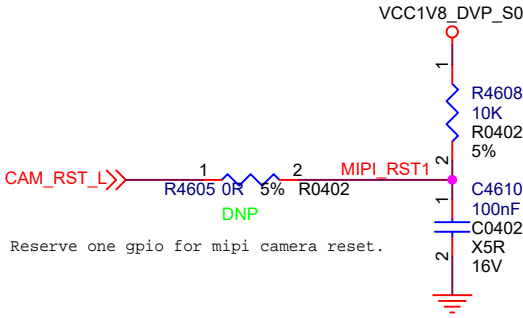
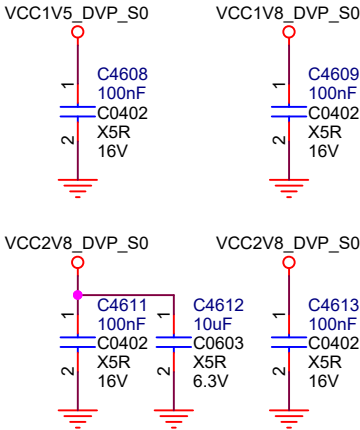
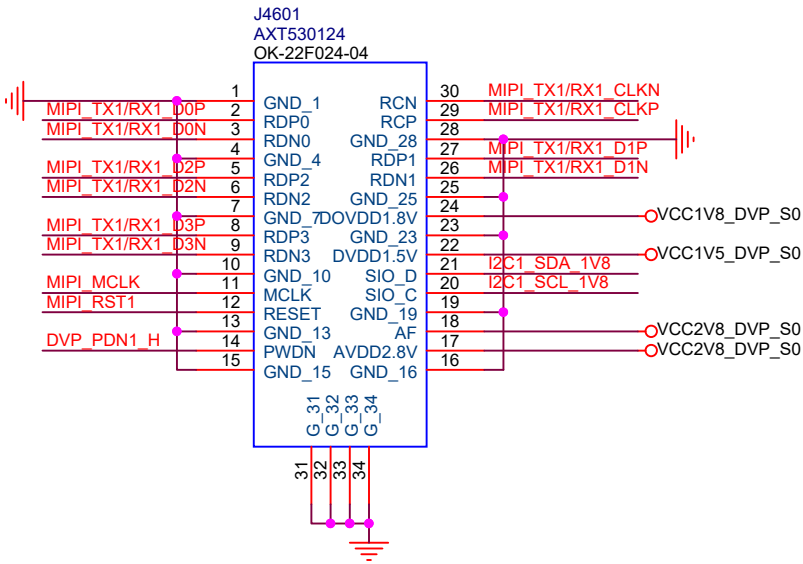



eMMC Flash

Note:Refer to the latest AVL for parts selection.



MIPI Camera



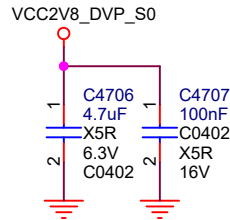
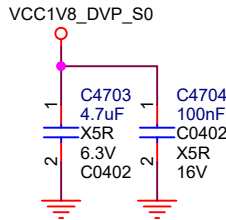
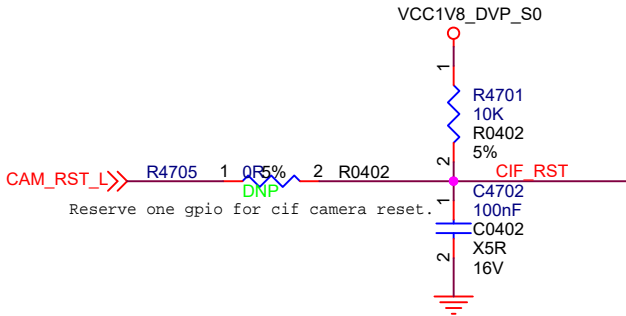
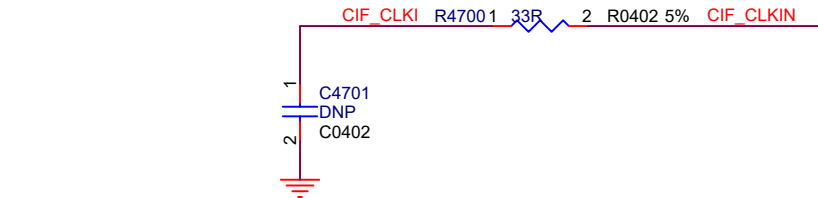
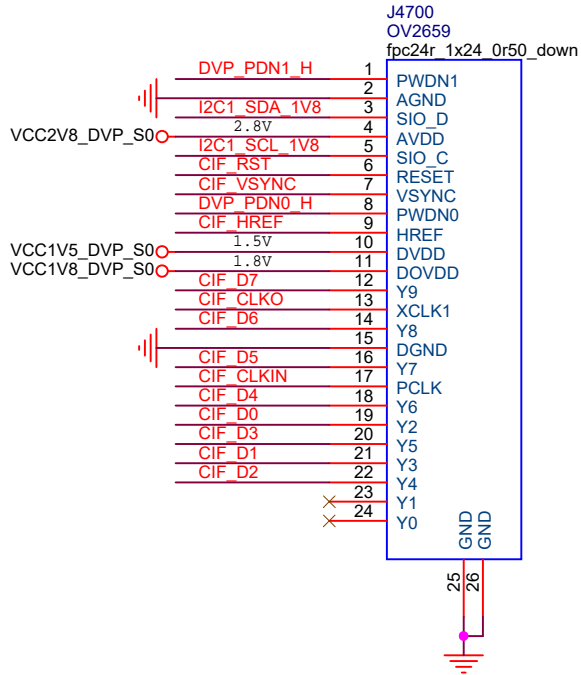
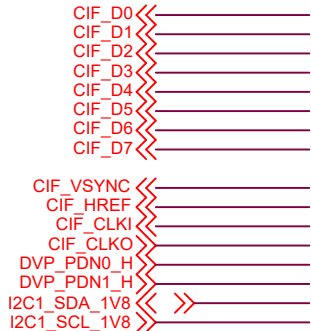


瑞芯微电子

Fuzhou Rockchip Electronics

Project:	RK3399Pro AI REF V11		
File:	46.Camera MIPI CSI		
Date:	Tuesday, May 21, 2019	Rev:	V1.1
Designed by:	Linus.Lin	Reviewed by:	<Checker>
		Sheet:	29 of 46

CIF Camera



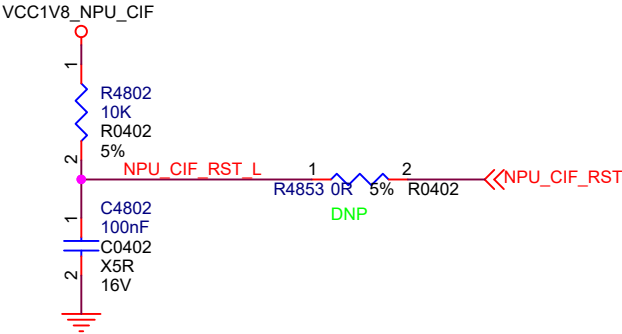
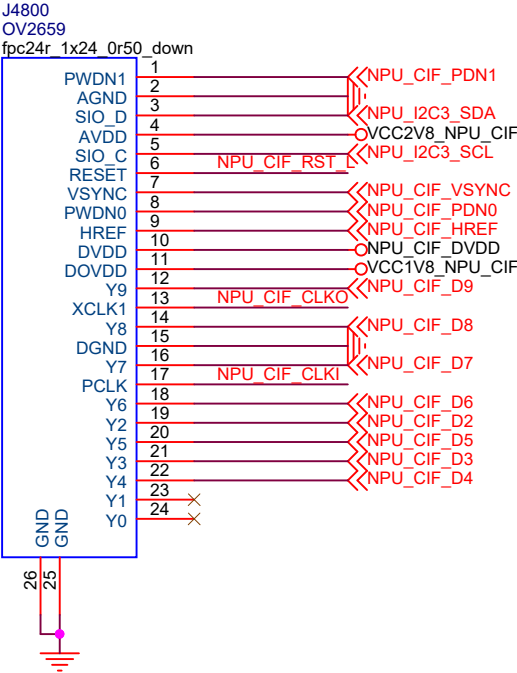
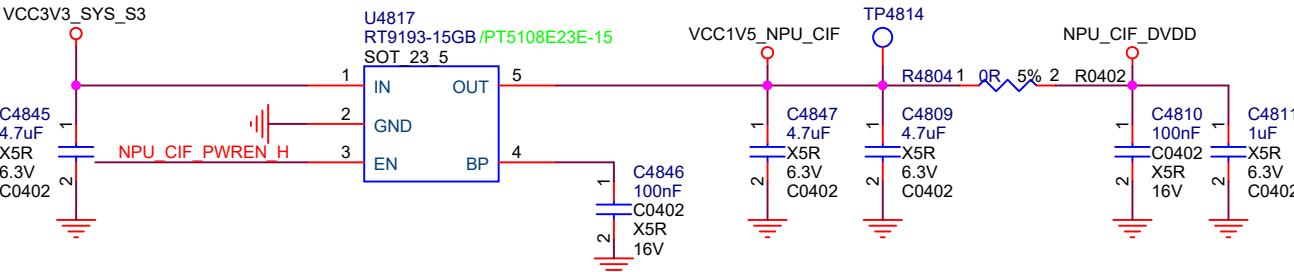
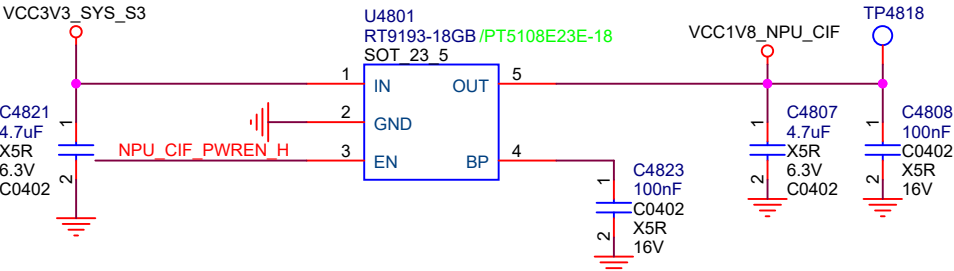
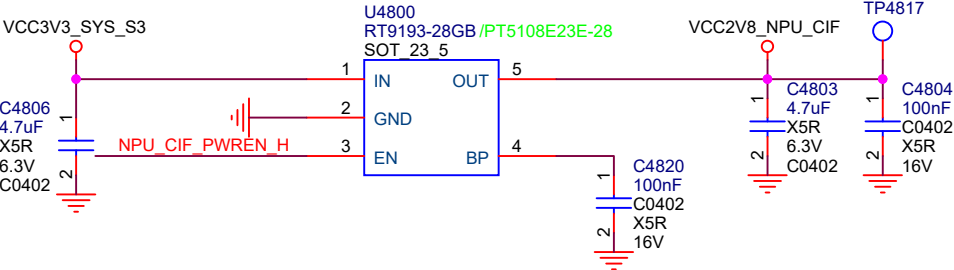
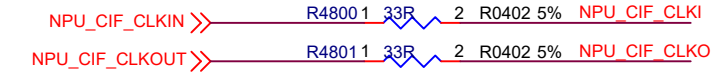
VCC1V5_DVP_S0 power circuit diagram:


- C4708 4.7uF, X5R 6.3V, C0402 connected to ground.
- C4709 100nF, C0402 X5R 16V connected to ground.

Note:

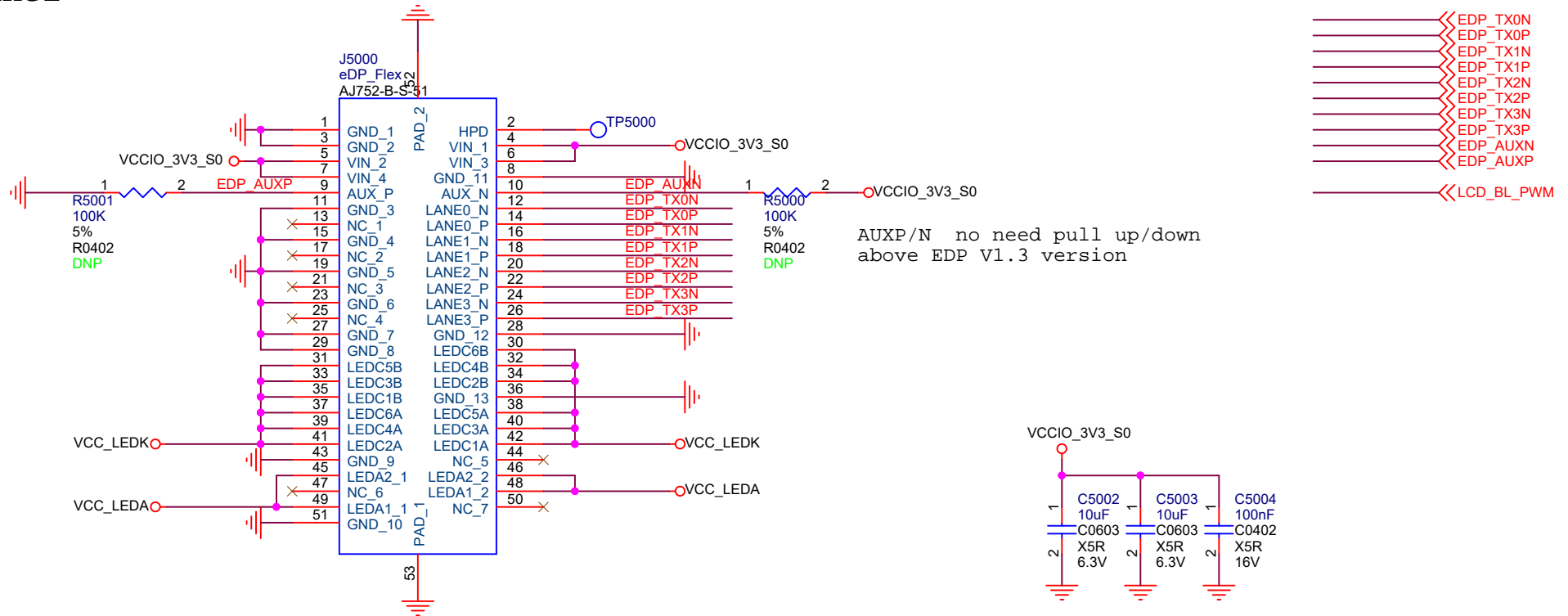
VDD1V5_DVP_S0 whether or not be power-on according to the type of camera module model and DOVDD power supply 请根据摄像头模组型号以及DOVDD供电情况, 来选择是否需要VDD1V5_DVP_S0电源供电。

NPU CIF Camera

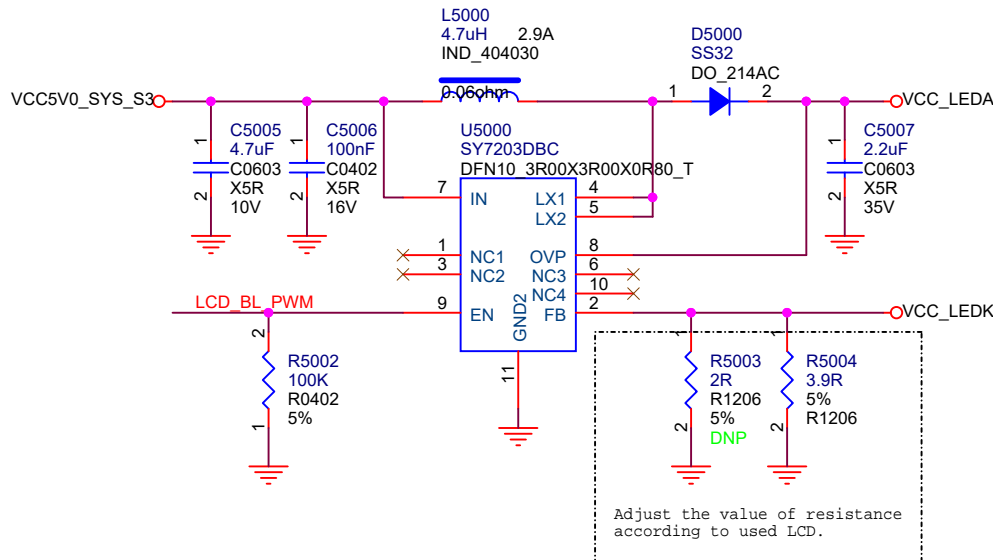


		Fuzhou Rockchip Electronics	
瑞芯微电子			
Project:	RK3399Pro AI REF V11		
File:	48.Camera NPU CIF		
Date:	Tuesday, May 21, 2019		Rev: V1.1
Designed by:	Linus.Lin	Reviewed by: <Checker>	Sheet: 31 of 46


eDP Panel



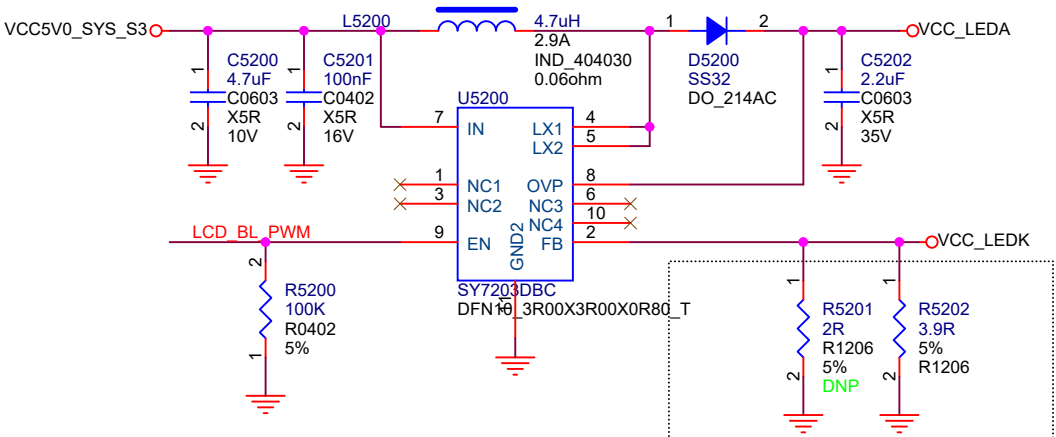
Backlight Power



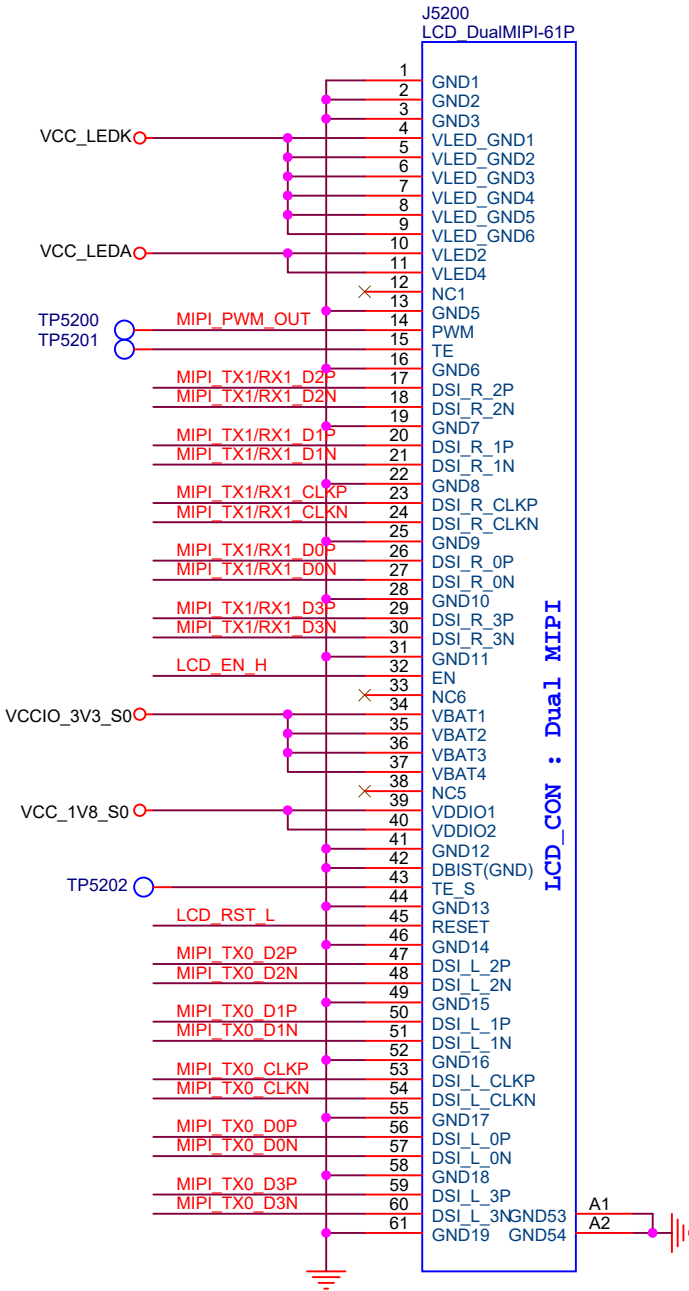
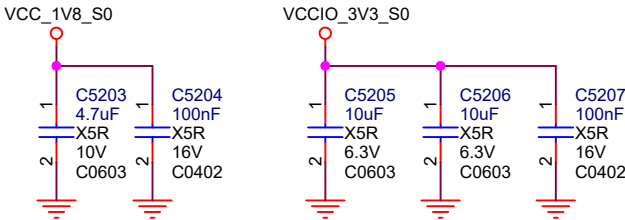
Note:
U5000 EN pin must support PWM brightness dimming control, Otherwise,
it needs to be increased PWM circuit at FB pin.
R5003&R5004 should be placed close to the power pins of Panel Interface.
U5000的EN管脚需要能支持PWM动态背光调节功能,
否则就需要在DCDC的FB管脚增加PWM电路来进行调节。
R5003&R5004必须靠近屏连接座的电源管脚放置而不是靠近DCDC放置。


 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399Pro AI REF V11		
File:	50.LCM eDP Panel		
Date:	Tuesday, May 21, 2019		Rev: V1.1
Designed by:	Linus.Lin	Reviewed by:	<Checker>
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Dual-MIPI LCM

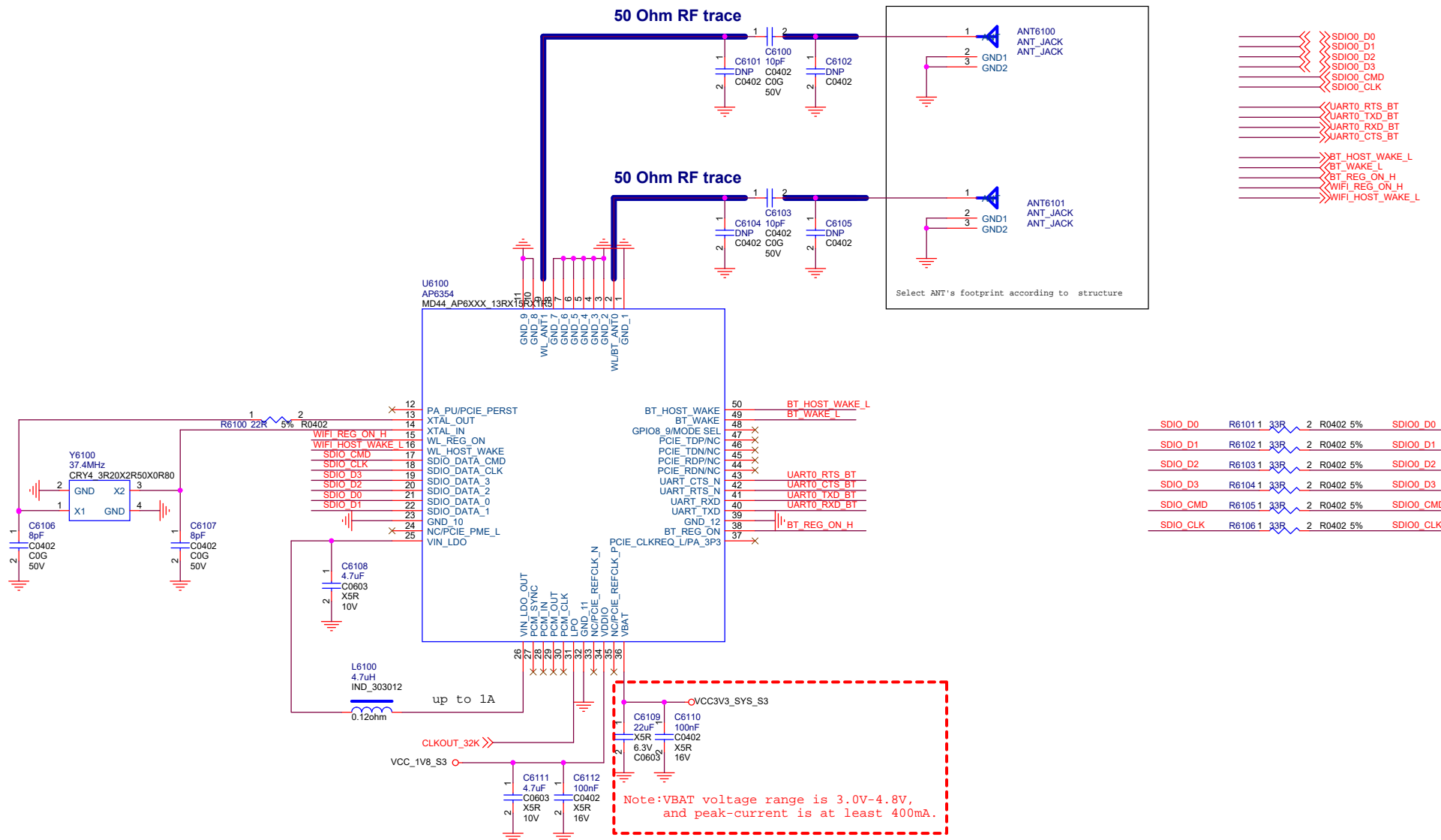


Note:
U5200 EN pin must support PWM brightness dimming control, Otherwise, it needs to be increased PWM circuit at FB pin.
R5201&R5202 should be placed close to the power pins of Panel Interface.
U5200的EN管脚需要能支持PWM动态背光调节功能, 否则就需要在DCDC的FB管脚增加PWM电路来进行调节。
R5201&R5202必须靠近屏连接座的电源管脚放置而不是靠近DCDC放置。



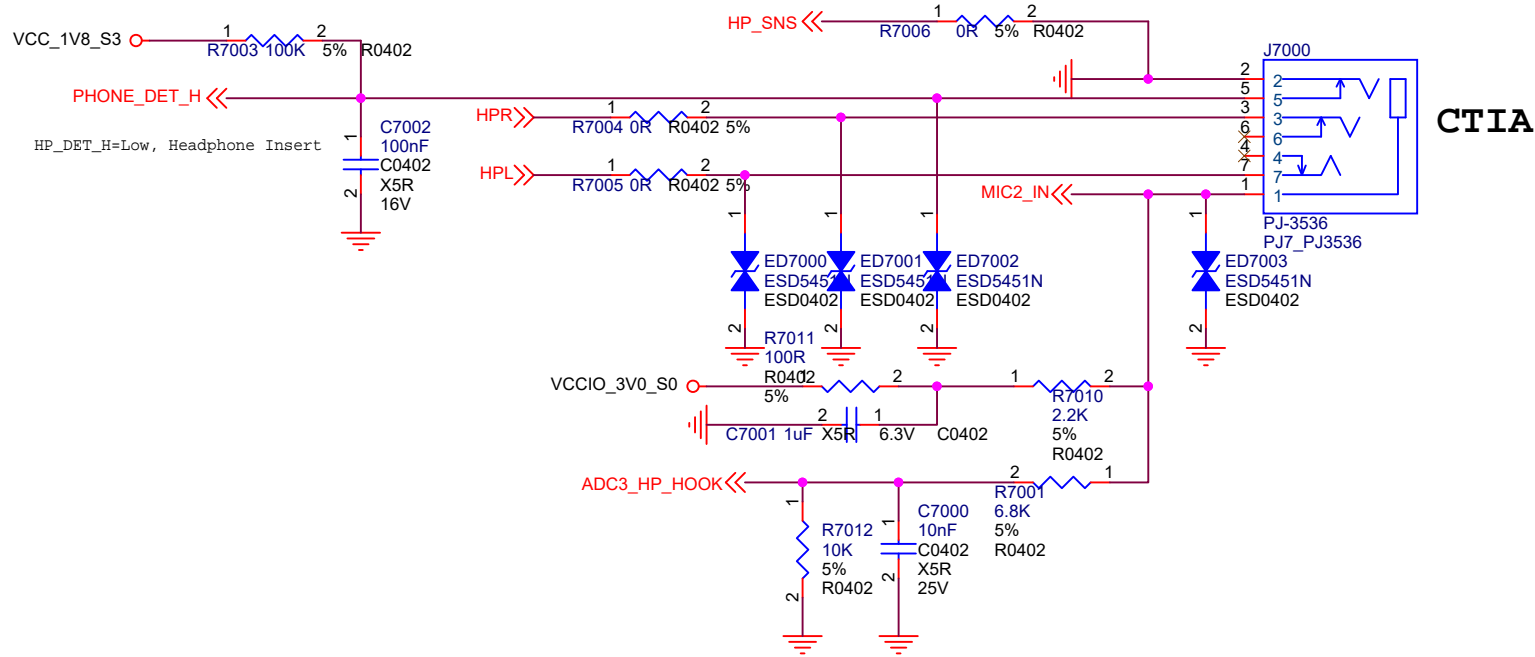
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Project:	RK3399Pro AI REF V11		
File:	52.LCM Dual MIPI(option)		
Date:	Tuesday, May 21, 2019	Rev:	V1.1
Designed by:	Linus.Lin	Reviewed by:	<Checker>
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SDIO WIFI/BT-2T2R

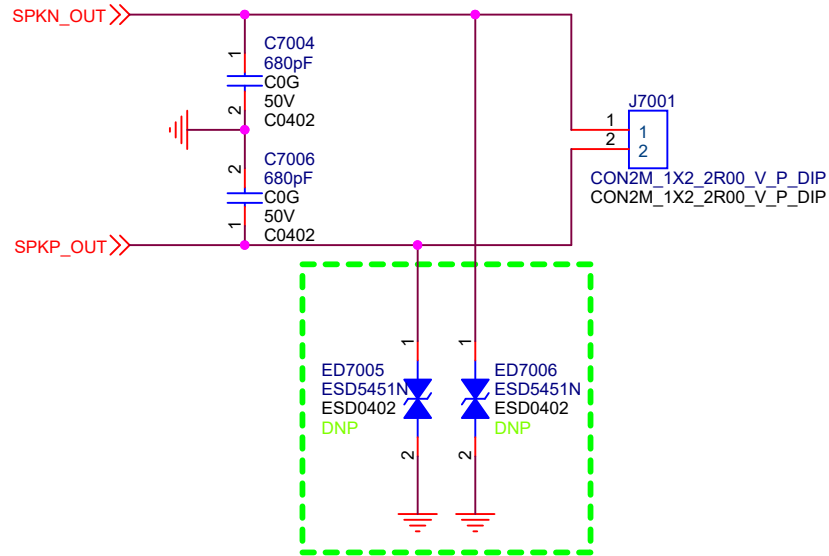


OPTION	WIFI				SRR	RSD	BT	Crystals	VCCIO_SDIO
	ax	ac	a	b/g/n					
AP62x2	No	No	Yes	Yes	No	No	4.0		1.8-3.3V
AP6356S	No	Yes	Yes	Yes	Yes	No	4.1		1.7-3.6V
AP6398S	No	Yes	Yes	Yes		Yes	5.0	37.4MHz	1.7-3.6V
AP6275S	Yes	Yes	Yes	Yes		Yes	5.0		

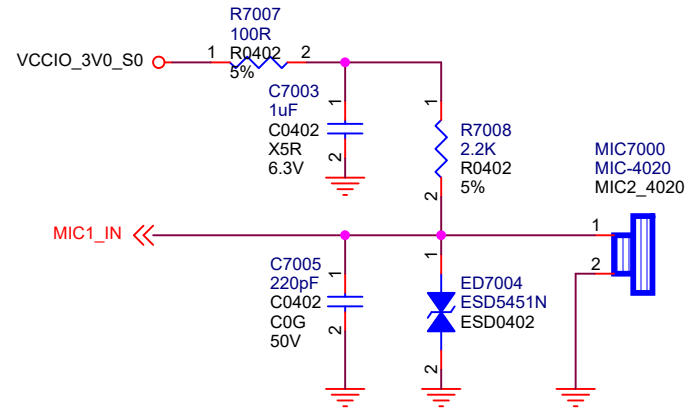
HEADPHONE




SPEAKER



MIC

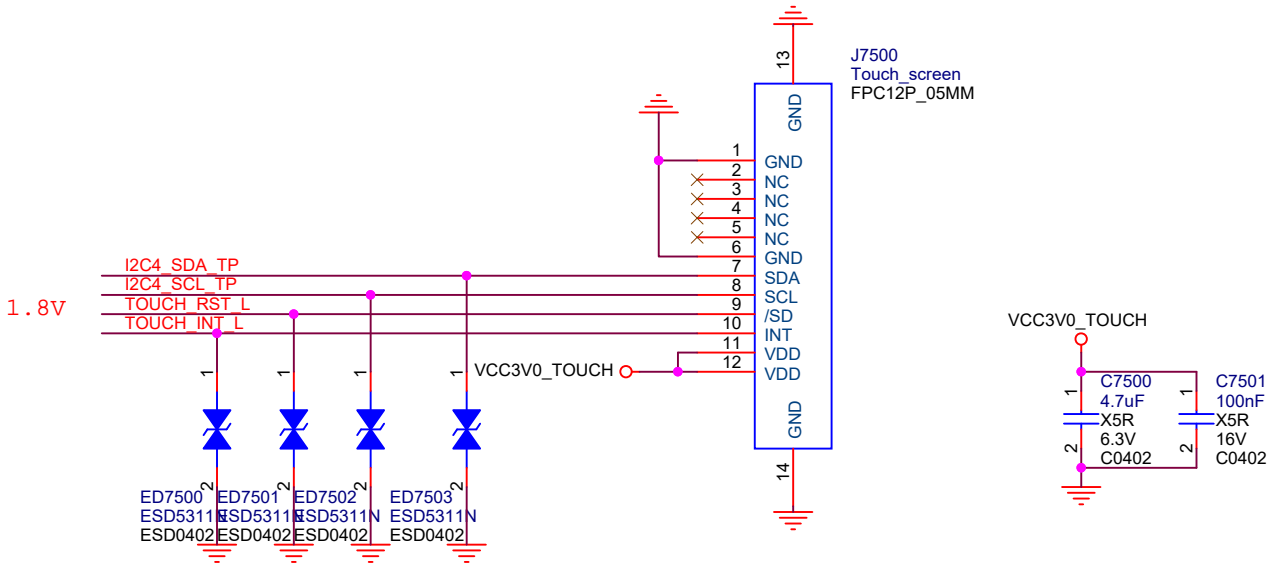


 瑞芯微电子		Fuzhou Rockchip Electronics			
Project:	RK3399Pro AI REF V11				
File:	70.AUDIO				
Date:	Tuesday, May 21, 2019			Rev:	V1.1
Designed by:	Linus.Lin	Reviewed by:	<Checker>	Sheet:	38 of 46

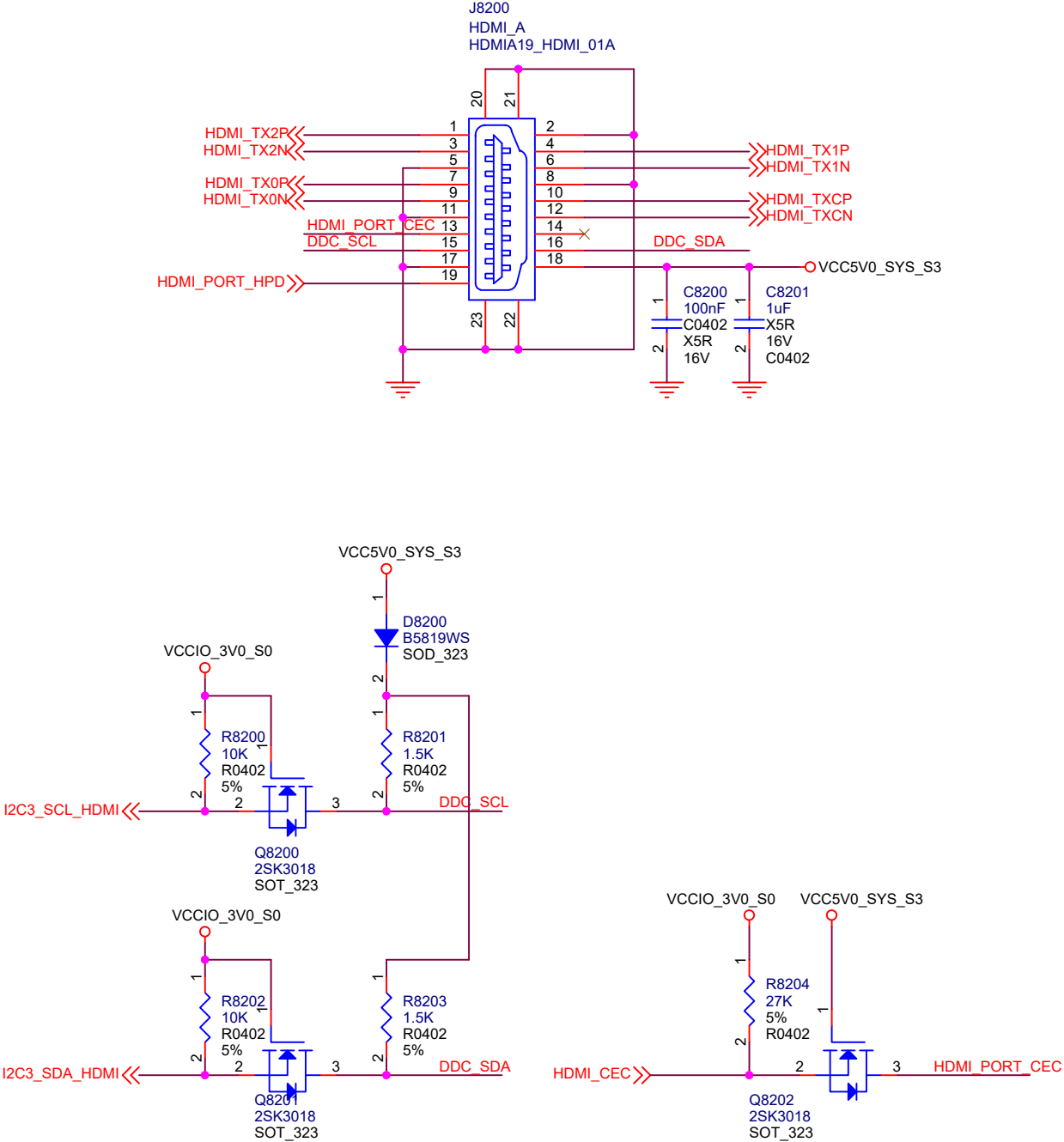
Touch Panel connector

Note:VDDIO of Touch Panel is 1.8V.

I2C4_SCL_TP
I2C4_SDA_TP
TOUCH_RST_L
TOUCH_INT_L

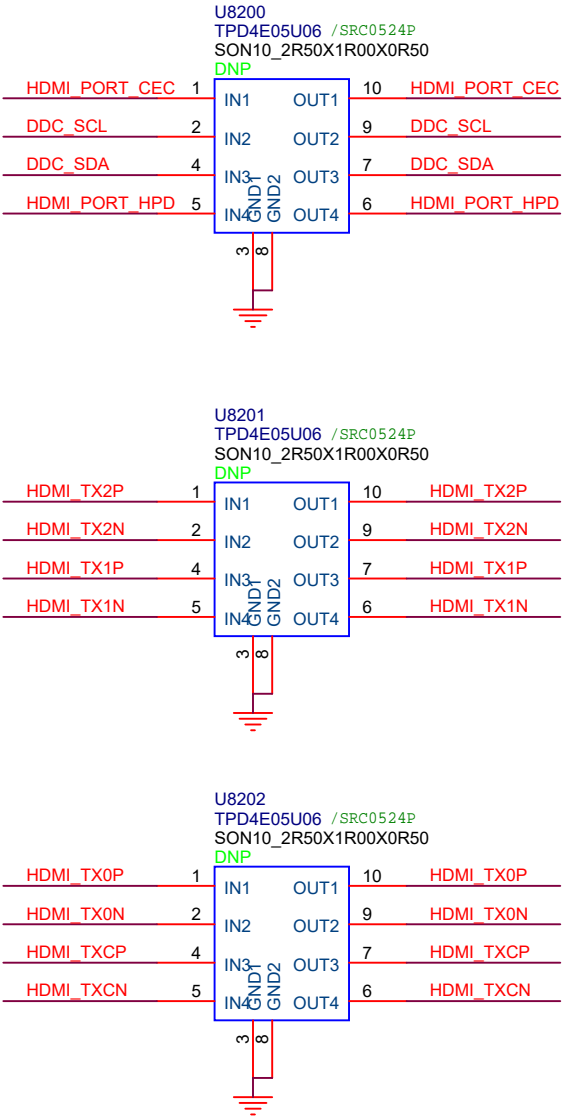



HDMI Port



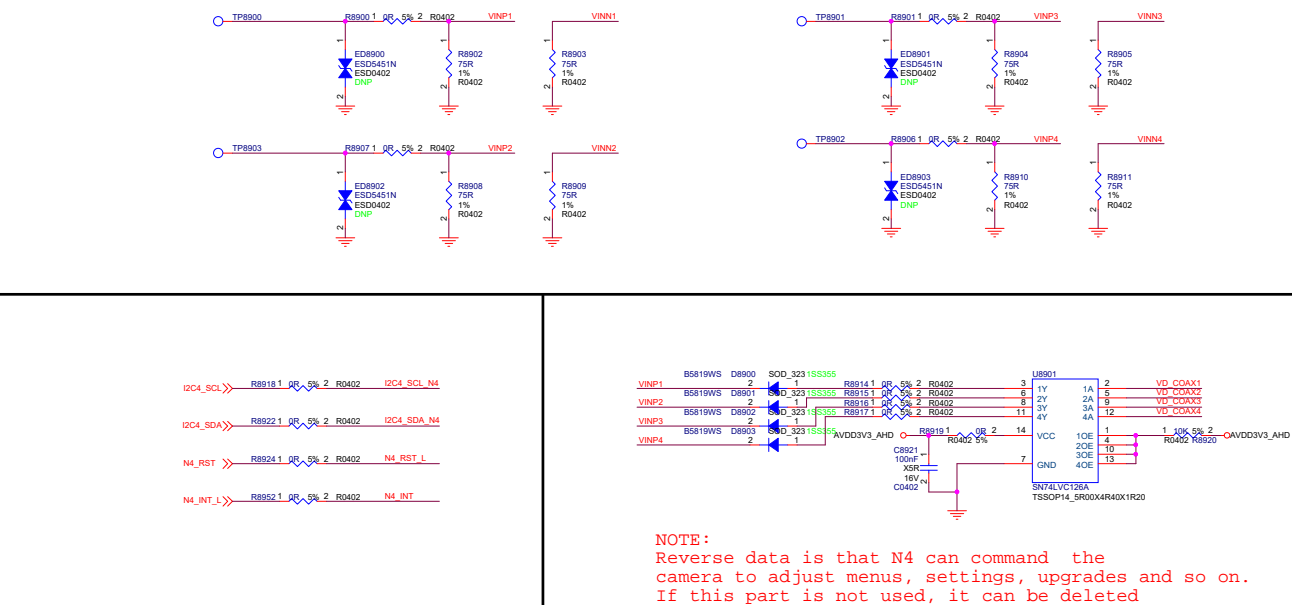
ESD

Note:All the ESD components should be placed close to the port and $C_j \leq 0.4\text{pF}$

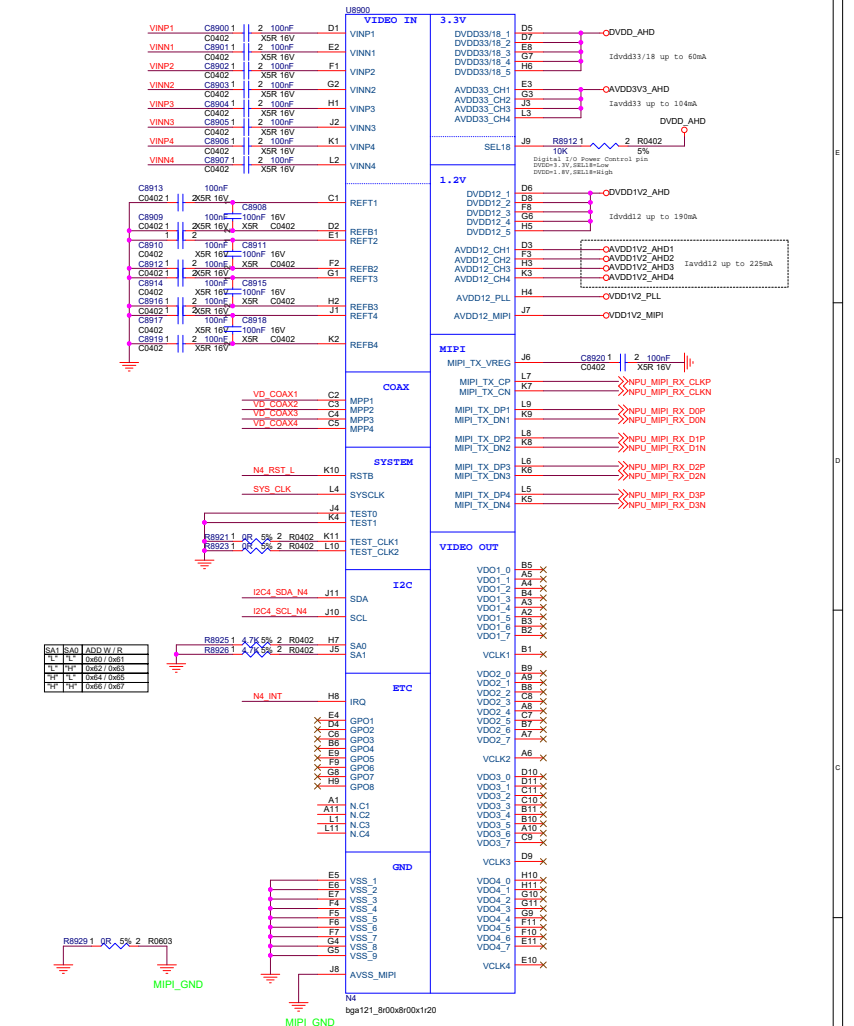
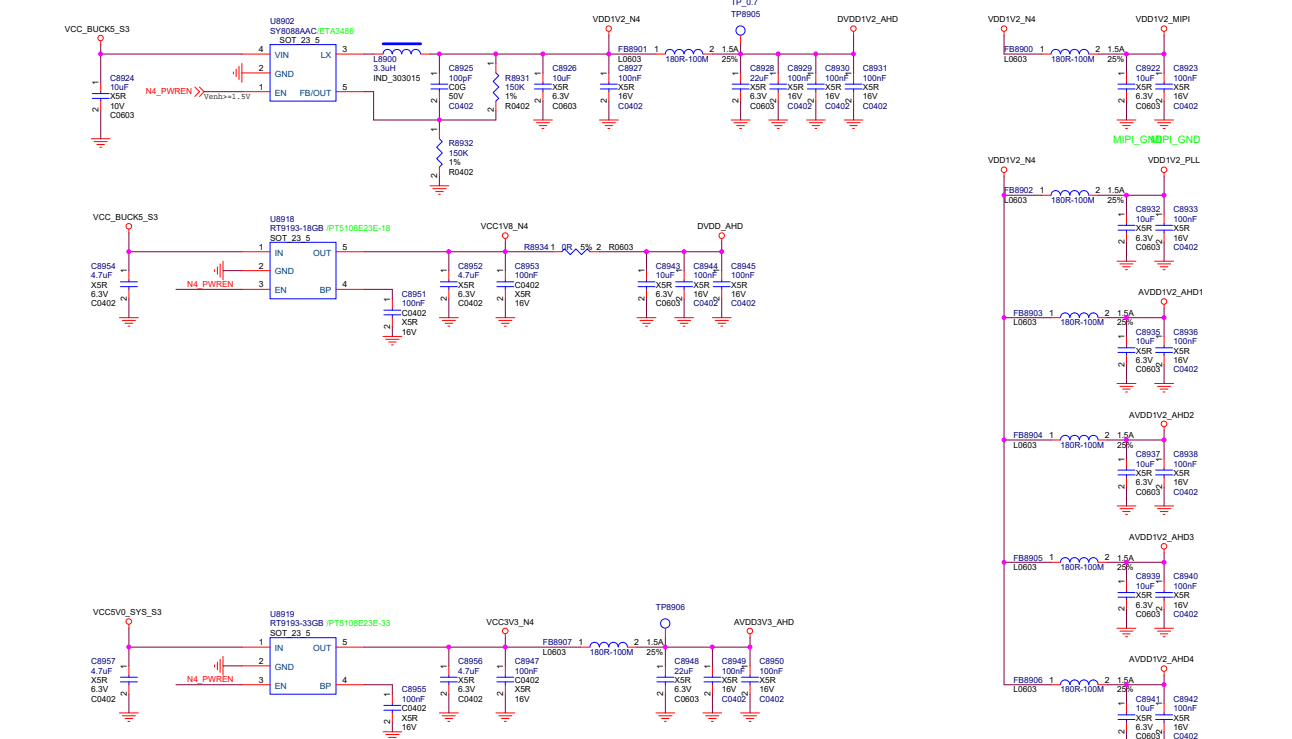


 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399Pro AI REF V11		
File:	82.HDMI Port		
Date:	Tuesday, May 21, 2019		Rev: V1.1
Designed by:	Linus.Lin	Reviewed by:	<Checker>
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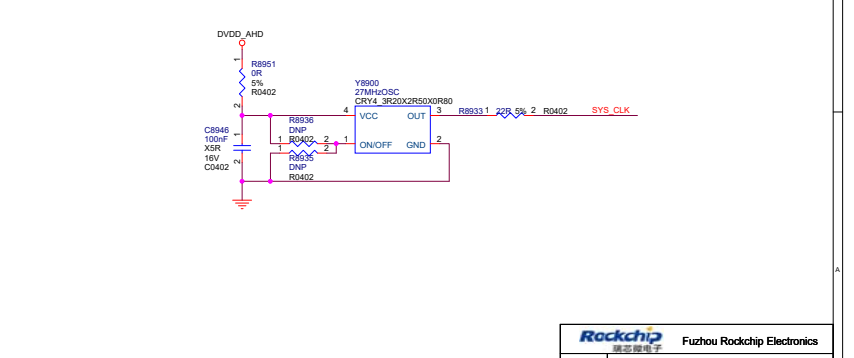
AHD Input



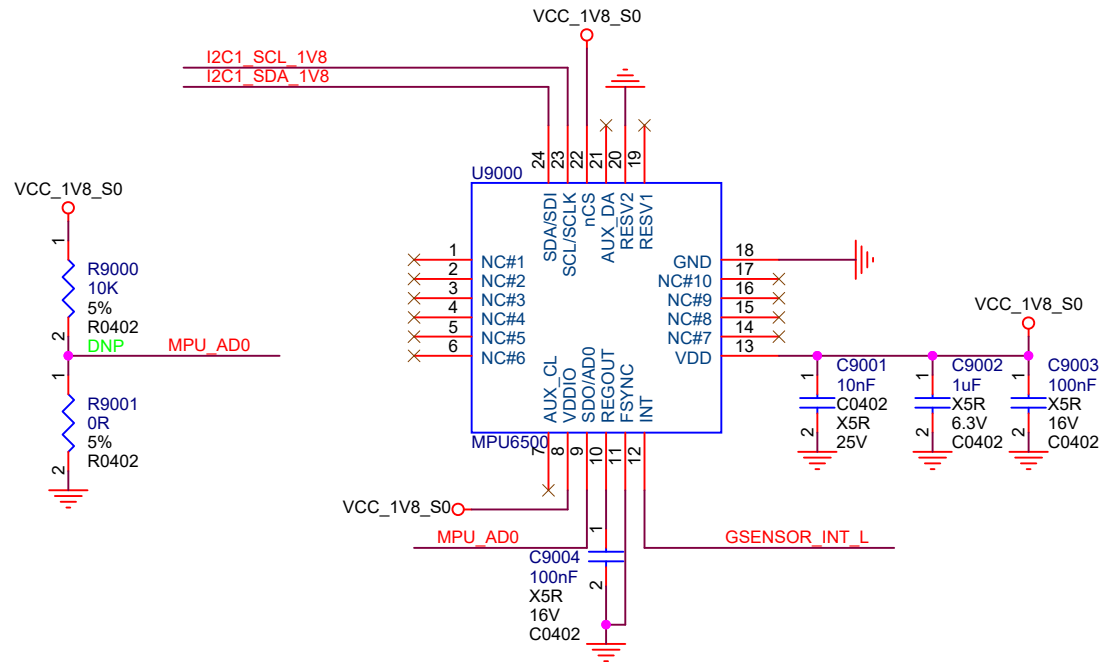
Power



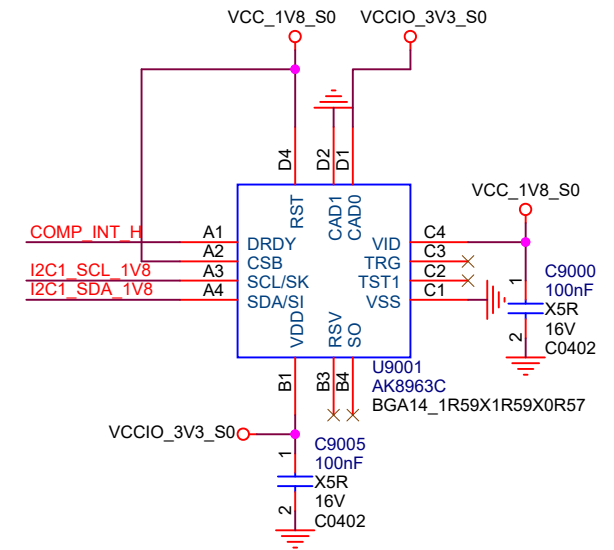
Clock



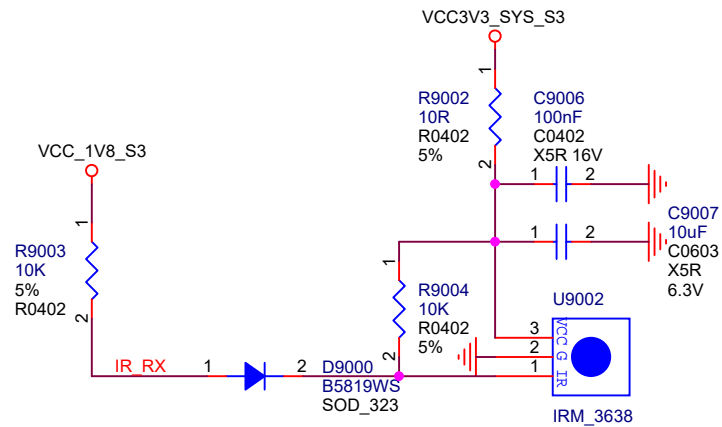
Gyroscope+G-sensor



Compass

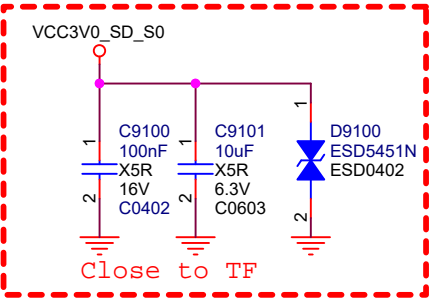
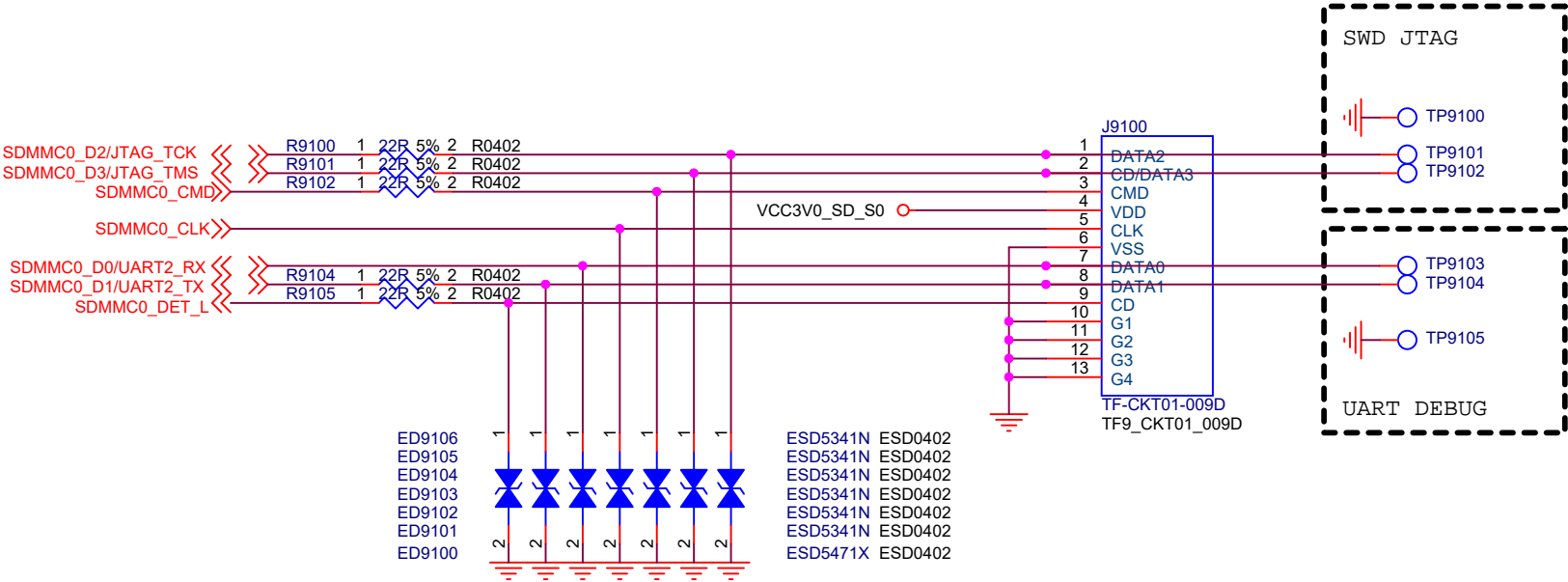



IR



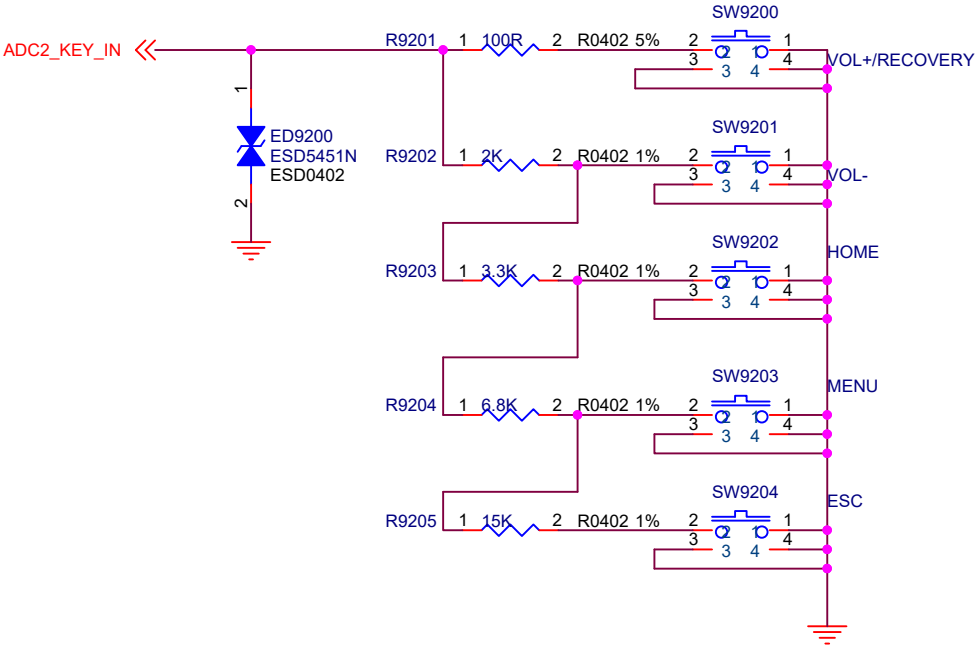
		Fuzhou Rockchip Electronics	
Project:		RK3399Pro AI REF V11	
File:		90.Sensor	
Date:	Tuesday, May 21, 2019	Rev:	V1.1
Designed by:	Linus.Lin	Reviewed by:	<Checker>
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TF Card



 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399Pro AI REF V11		
File:	91.TF Card		
Date:	Tuesday, May 21, 2019		Rev: V1.1
Designed by:	Linus.Lin	Reviewed by:	<Checker>
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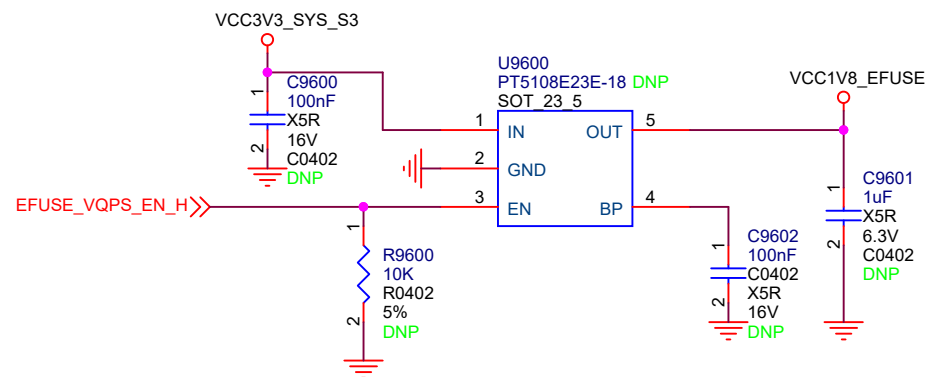
Key Array



Key Name	ADC Value
VOL+/RECOVERY	10
VOL-	170
HOME	354
MENU	560
ESC	747

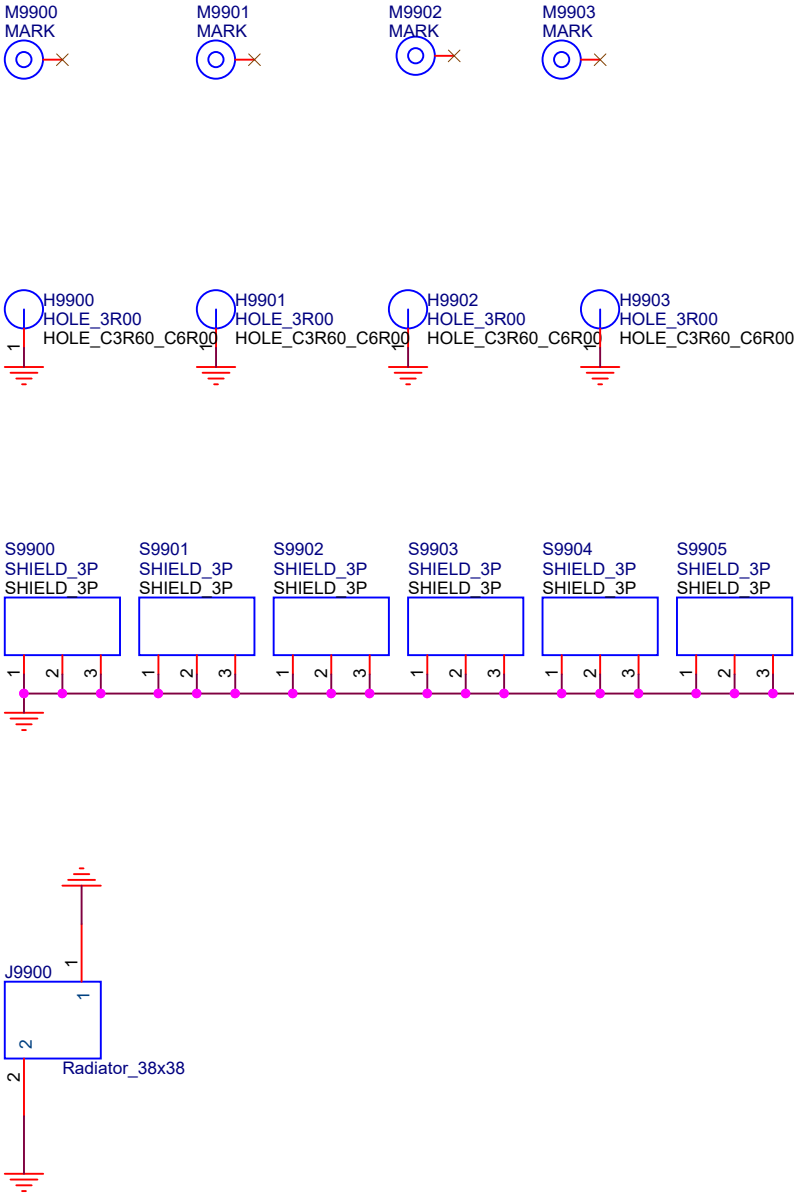
eFUSE(option)


Note:Power for eFUSE Program,it is recommended to reserve on the tooling.
It can be deleted if no need eFUSE function.



 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399Pro AI REF V11		
File:	96.eFUSE (option)		
Date:	Tuesday, May 21, 2019		Rev: V1.1
Designed by:	Linus.Lin	Reviewed by:	<Checker>
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MARK/HOLE/Heat Sink



 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399Pro AI REF V11		
File:	99.MARK/HOLE/Heat Sink		
Date:	Tuesday, May 21, 2019		Rev: V1.1
Designed by:	Linus.Lin	Reviewed by: <Checker>	Sheet: 46 of 46